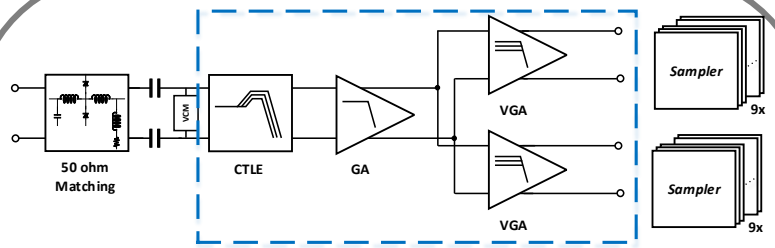
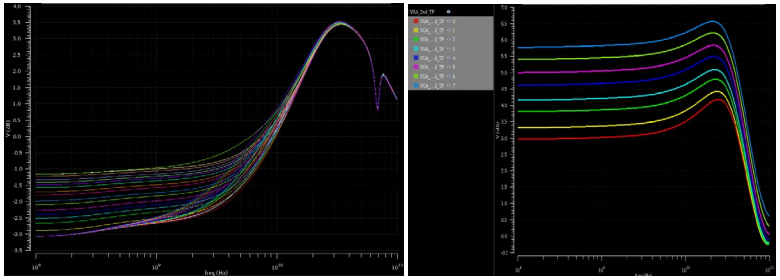
2020-2 ~ 2021 Works

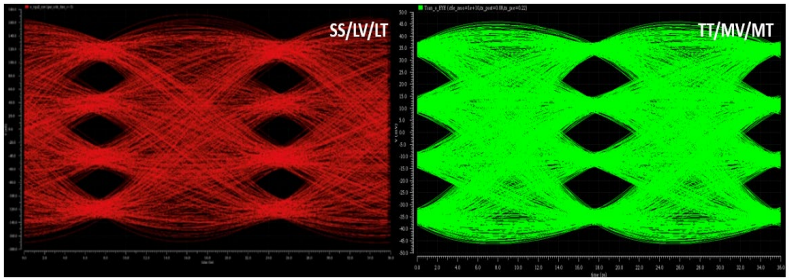
112Gb/s SerDes - Intern



[Block Diagram]

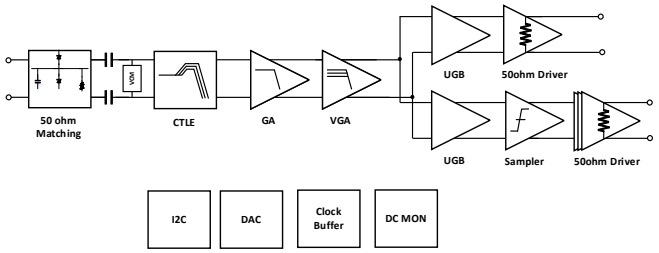


[CTLE & VGA Transfer Function]

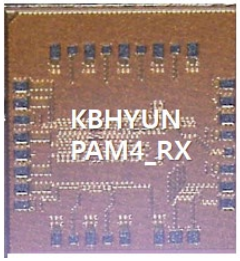


[Analog Front-End Output]

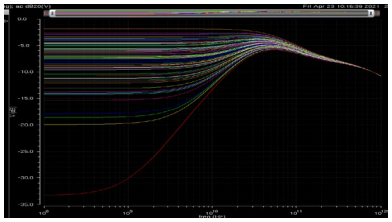
100Gbps PAM-4 Receiver Analog Front-End in 28nm



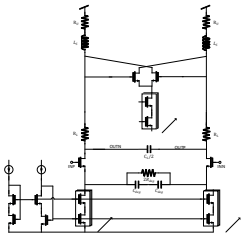
[Block Diagram]

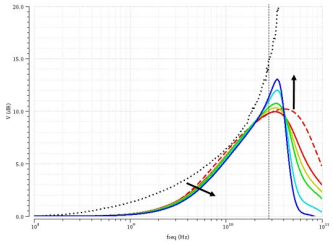


[Chip Photo]



[AFE Transfer function]

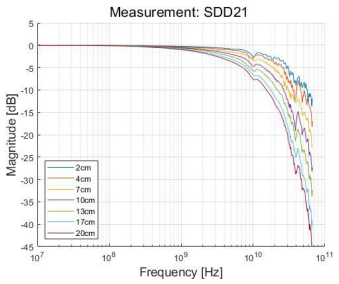


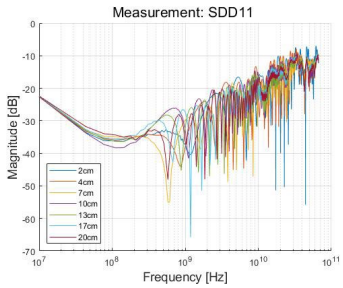


[CTLE Transfer function]

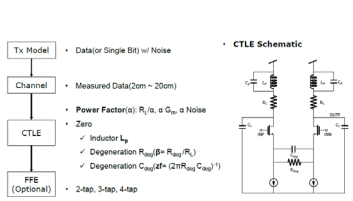
2022 Works

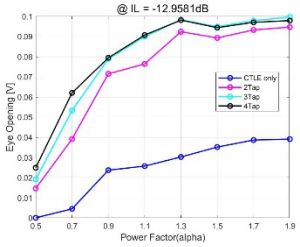
Channel Equalization

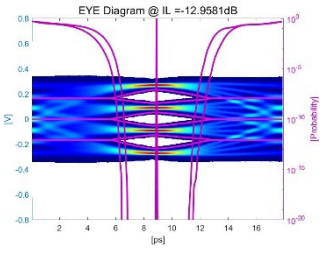


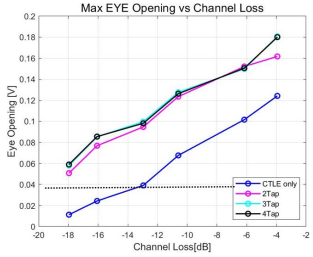


[Channel Measurement]



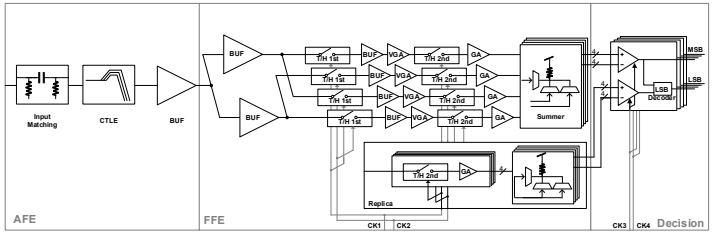


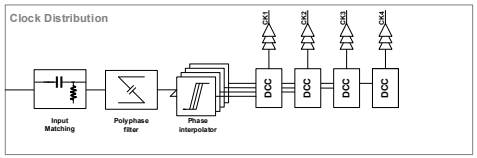




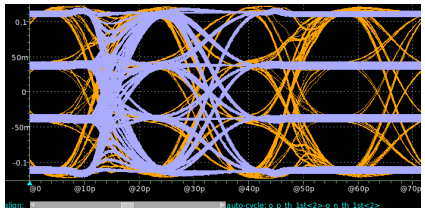
[Matlab Behavioral Modeling]

100Gbps PAM-4 Receiver Using Time-Based LSB Decoder and 3-Tap FFE





[Top Block diagram]



[FFE eye diagram]

	This	ISSCC'22	ISSCC'21	ISSCC'21	ISSCC'19
Tech	28nm	28nm	7nm	7nm	14nm
Data rate	100	112	112	106.25	100
Modulation	PAM4	PAM4	PAM4	PAM4	PAM4
Rx	Mixed	Mixed	Mixed	Mixed	Mixed
Tx	-	Mixed	5b DAC	5b DAC	8b DAC
Loss at Nyq	16	20.8	7	10	19.2
BER	-	<1e-11	1.30E-10	<1e-10	<1e-12
Efficiency	2.48 (Rx only)	2.29	1.7	1.45	3.7
Tx FFE	-	3-tap	5-tap	3-tap	8-tap
Rx FFE	3-tap	4-tap	-	-	-
Rx DFE	-	-	-	-	1-tap
Rx inductor	Yes	No	Yes	Yes	Yes

[Comparison table]

2022~ Plan

- Measurement
  - SEC 2204:
    - 100Gbps PAM-4 Receiver Using Time-Based LSB Decoder and 3-Tap FFE

- Design
  - SEC 2210:
    - 56Gb/s PAM-4 Receiver