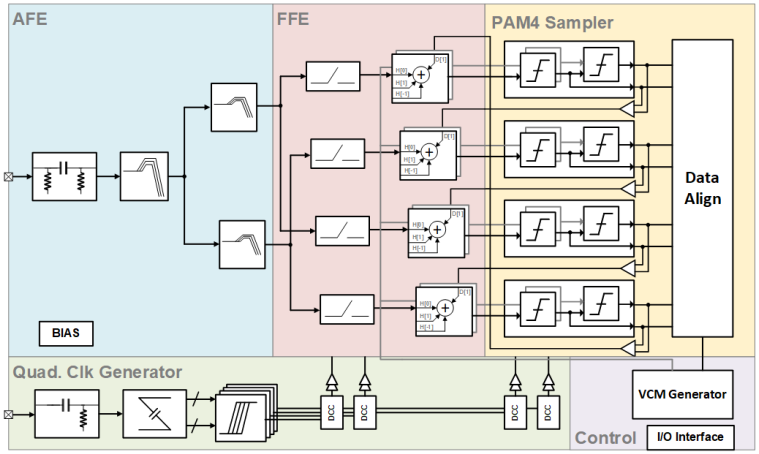
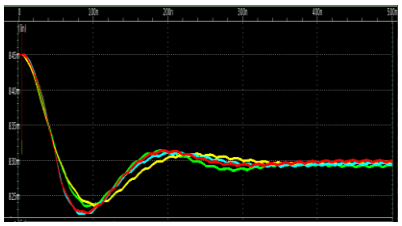
2022 ~ 2023 Works

56Gbps PAM-4 Rx with 3-Tap FFE and reference voltage calibration loop



[Top Block diagram]

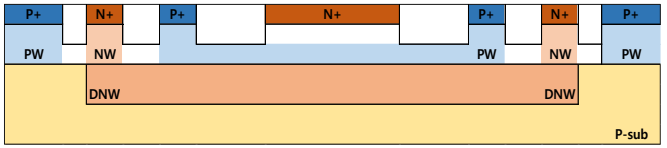


[Calibration loop]

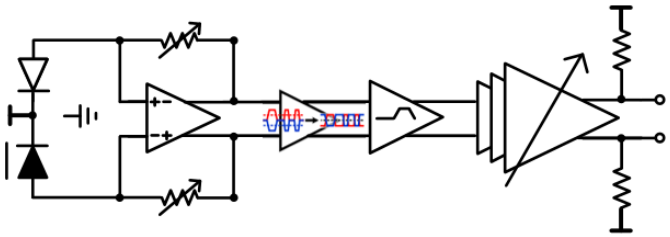
		[1]	[2]	[3]	[4]
	This, SEC2210	JSSC'22	JSSC'21	JSSC'19	JSSC'22
Tech	28nm CMOS	28nm CMOS	28nm CMOS	28nm FDSOI	7nm FinFET
Data rate	56	56	60	64	112
Modulation	PAM4	PAM4	PAM4	PAM4	PAM4
Rx	Mixed	Mixed	Mixed	Mixed	7b ADC
Tx	-	-	-	Mixed	-
Loss at Nyq(dB)	20	9.68	8.2	16.8	36
Efficiency(pJ/b)	1.51	0.975	1.1	2.8	1.741*
Efficiency/loss	0.0755	0.1007	0.1341	0.1666	0.0483
Tx FFE	-	-	-	4-tap	-
Rx FFE	3-tap	-	-	-	5
Rx DFE	-	-	2-tap	-	9
Rx Inductor	No	No	No	No	No

[Comparison table]

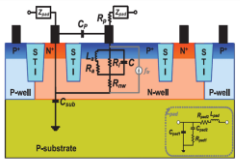
CMOS 28nm APD and monolithic receiver



[APD Cross section]

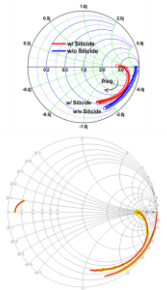


[ORx block diagram]



Myung-Jae Lee, Electron DEVICE LETTERS, 2016

	28nm CMOS	130nm CMOS
Rp [ohm]	0	0
Cp [fF]	3	60
La [nH]	11	13
Ra [ohm]	150	120
Rl [kohm]	5	1.2
C [fF]	33	140
Rnw [ohm]	140	70
Csub [fF]	7	45
ftr [GHz]	3.2	3



[APD Modeling]

2023~ Plan

- Measurement
  - SEC 2210:
    - 56Gbps PAM-4 Rx with 3-Tap FFE and reference voltage calibration loop
  - SEC 2301
    - APD ORx

- Design
  - SEC 28nm
    2023.04 (APD ORx), 2023.10(High speed Rx)