2023 Workshop

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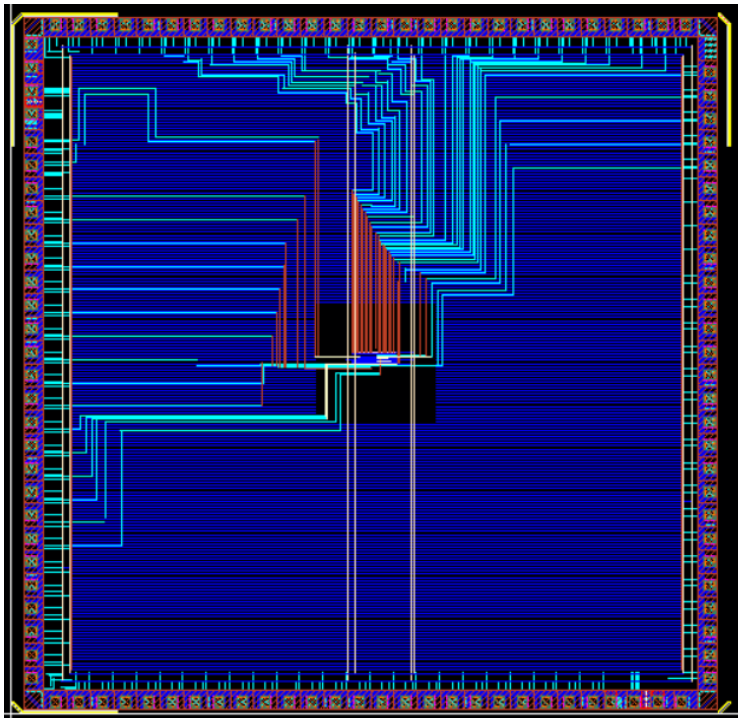
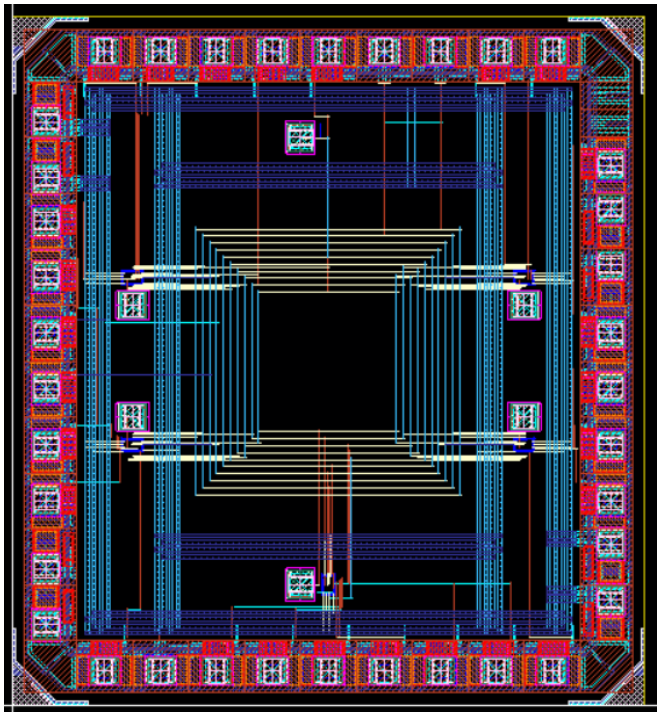
2023-1 Works

2 Tape-OUT



Vernier Delay Line TDC



SPAD AFE with PHS

2023-2 Plan

- **90nm Chip Measurement Environment Setup (FPGA)**
- **RTL Design (Using Verilog)**