

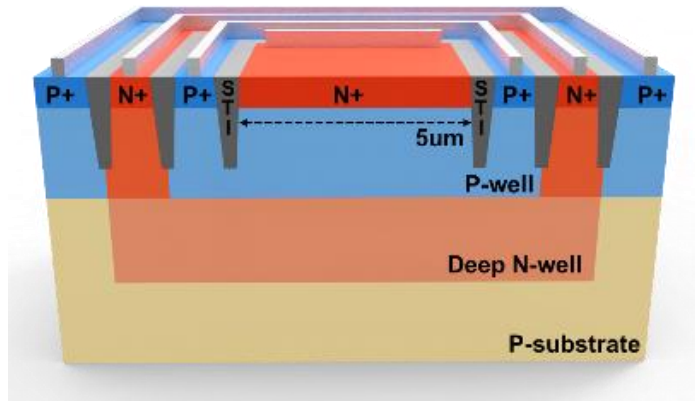
The background features a large, light blue watermark of the Yonsei University logo. The logo is circular with the text 'YONSEI UNIVERSITY' around the top and '1885' at the bottom. In the center is a shield with a book, a lamp, and a central circle.

2023 Workshop

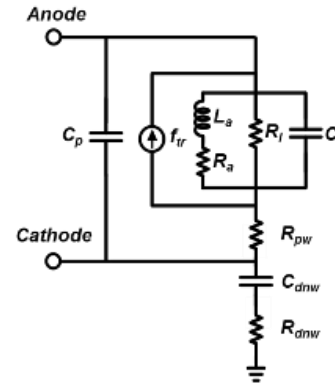
SeunegJae Yang

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Dept. of Electrical and Electronic Engineering
Yonsei University**

CMOS 28nm APD ORx

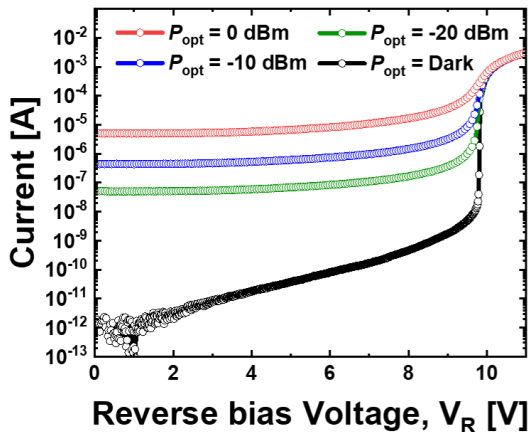


APD Cross section

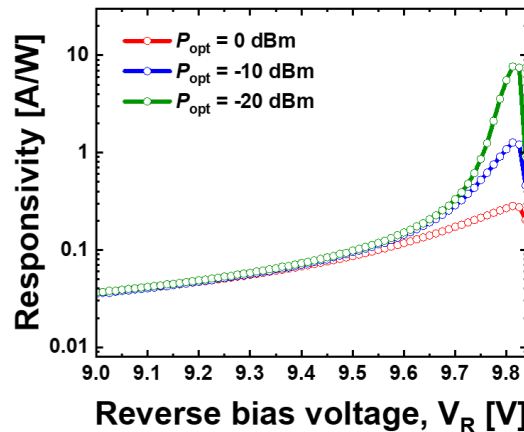


| | 9.4V | 9.8V | 10.2V |
|------------------------|-------|------|-------|
| C_p [fF] | 5 | | |
| L_a [nH] | 20 | 14 | 4.3 |
| R_a [Ω] | 12800 | 825 | 240 |
| R_i [k Ω] | 20 | 12 | 8 |
| C_j [fF] | 19 | 16 | 12 |
| R_{pw} [Ω] | 100 | | |
| R_{dnw} [Ω] | 220 | | |
| C_{dnw} [fF] | 190 | 165 | 140 |
| f_{tr} [GHz] | 5.8 | 5.9 | 9 |

APD Modeling

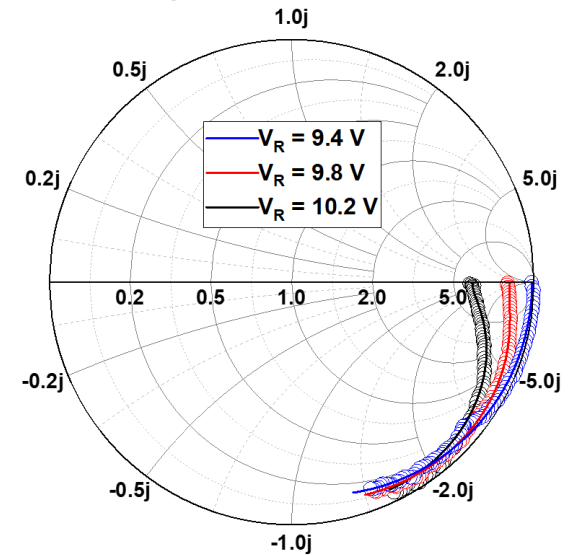


(a)

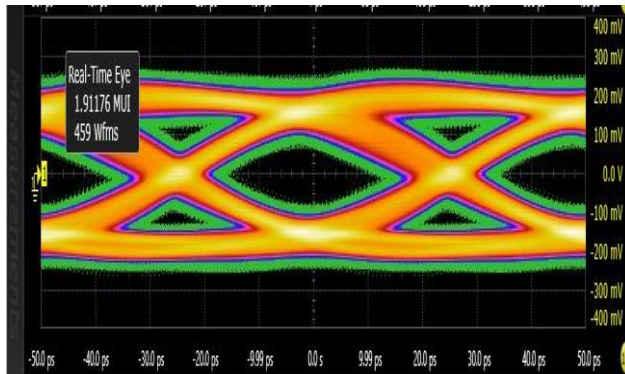
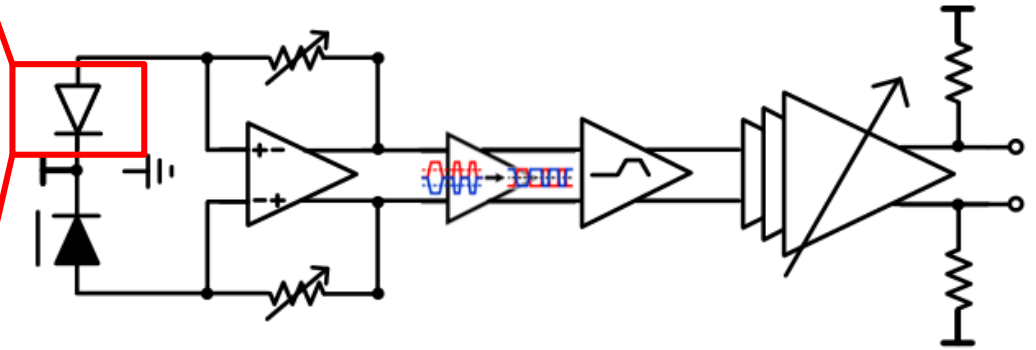
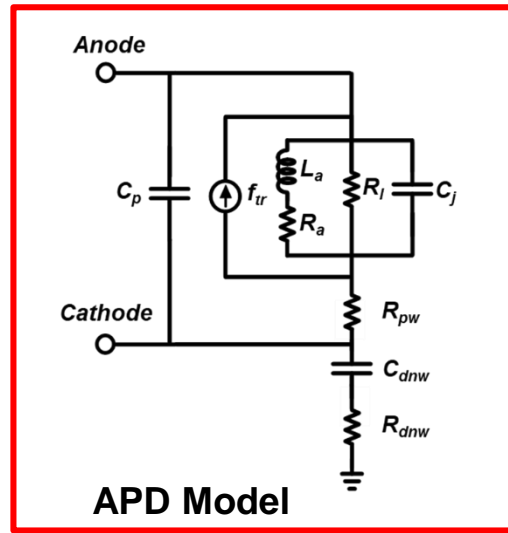


(b)

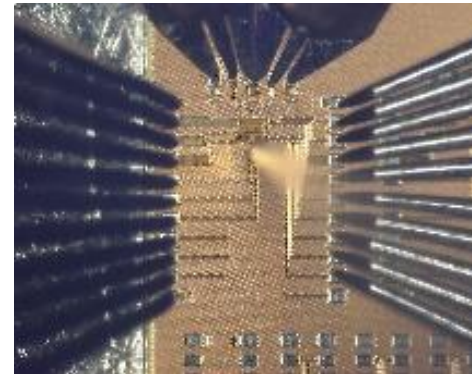
APD Measurement



CMOS 28nm APD ORx

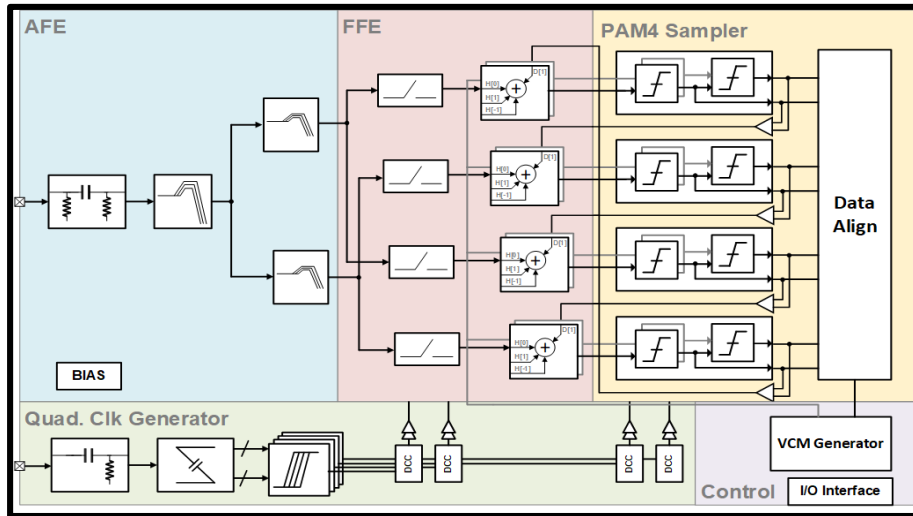


20Gbps eye diagram

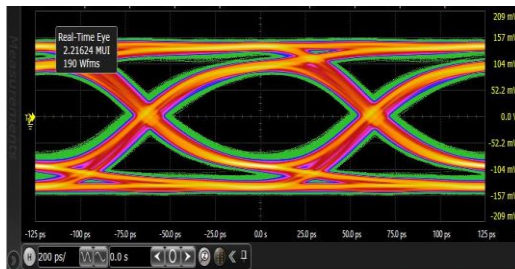


Chip photo

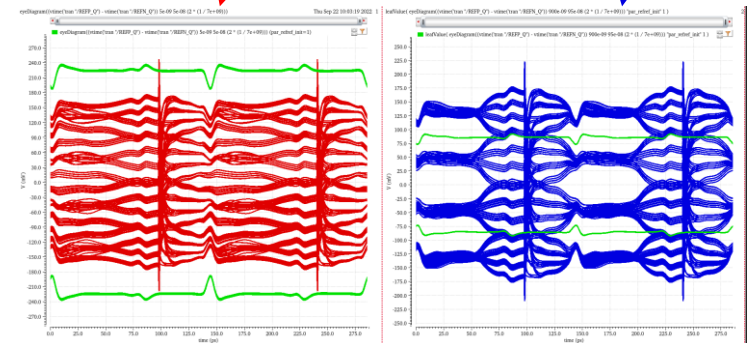
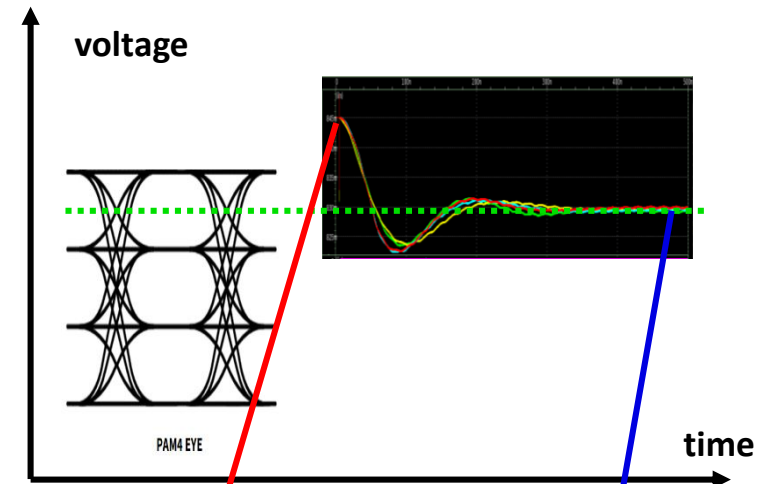
56Gbps* PAM-4 Rx w/ FFE & DFE



Top Block diagram



32Gbps* NRZ eye diagram



PAM4 reference calibration

2023~ Plan

➤ Measurement

– SEC 2307

- APD ORx with on-chip reverse bias control loop

➤ Internship

– IMEC 23.09 ~ 23.11

- Effect of EIC/Packaging technology scaling analysis