2023-2

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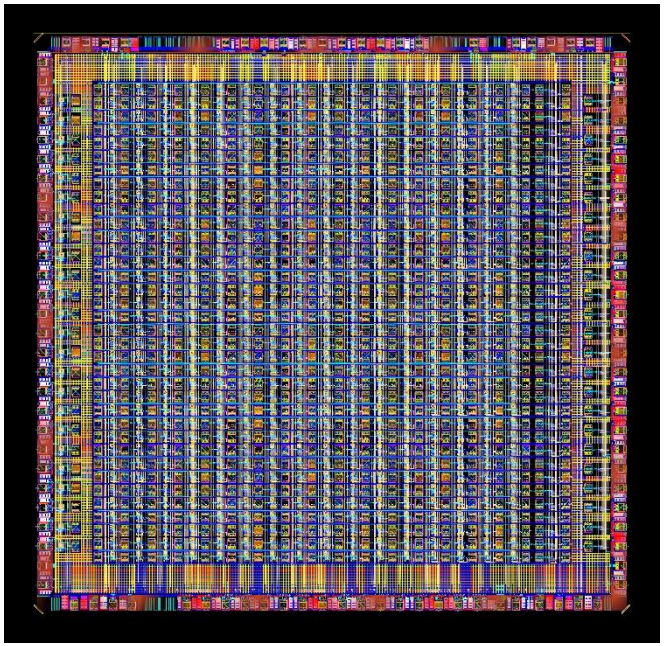
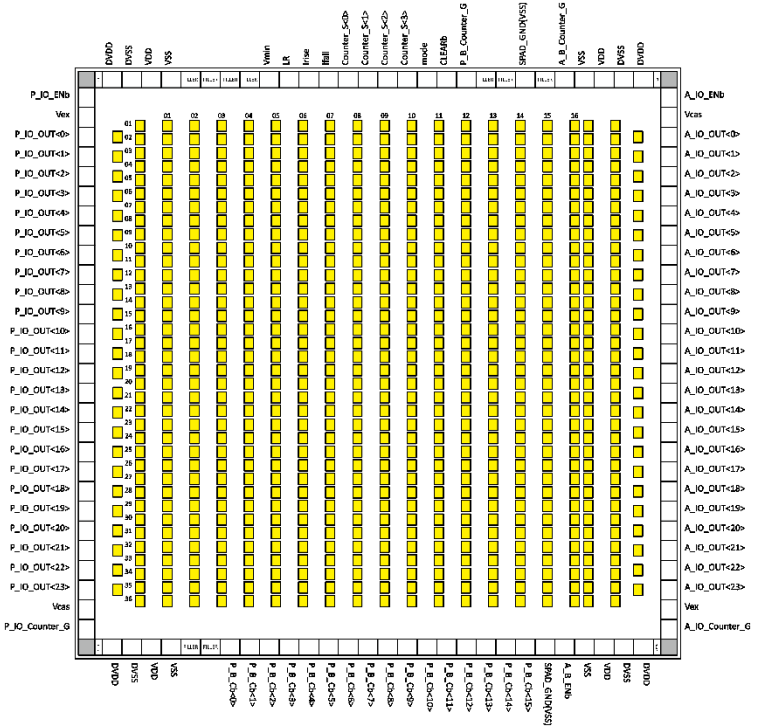
Achievements

- **Process** : DBH 90nm CIS (BSI)
- **Area** : 4,460um × 4,350um
- **Design** : SPAD AFEs

- **Purpose**
  1) Detect sub-ns output pulse.
  2) Verify differences about output characteristic between 'I/O Pad' and 'Bond Pad'
  3) Designed SPAD verification.

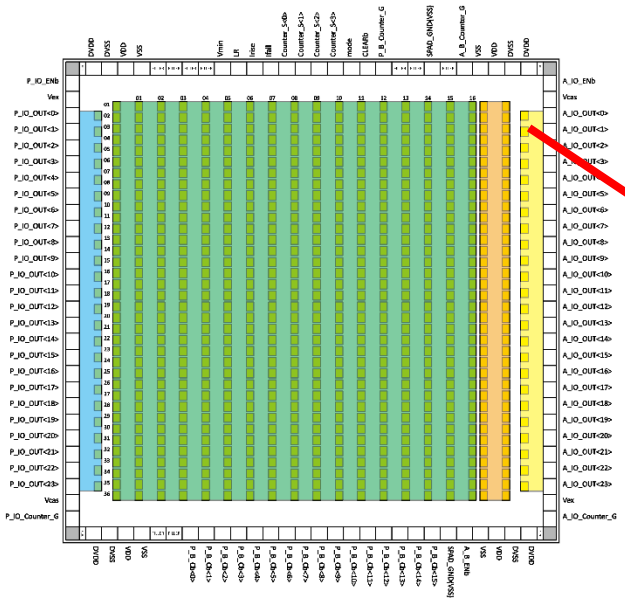


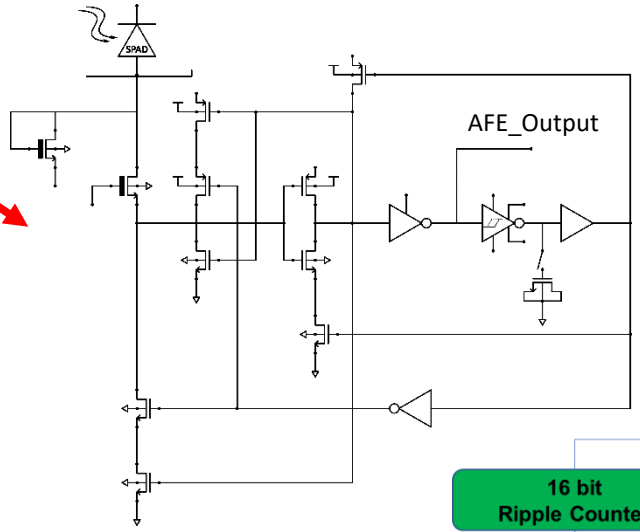
<TOP View>



<TOP Concept View>

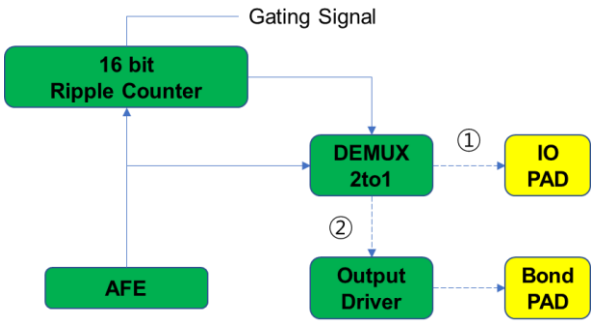
Achievements





<SPAD AFE>

<Read-out Stage>

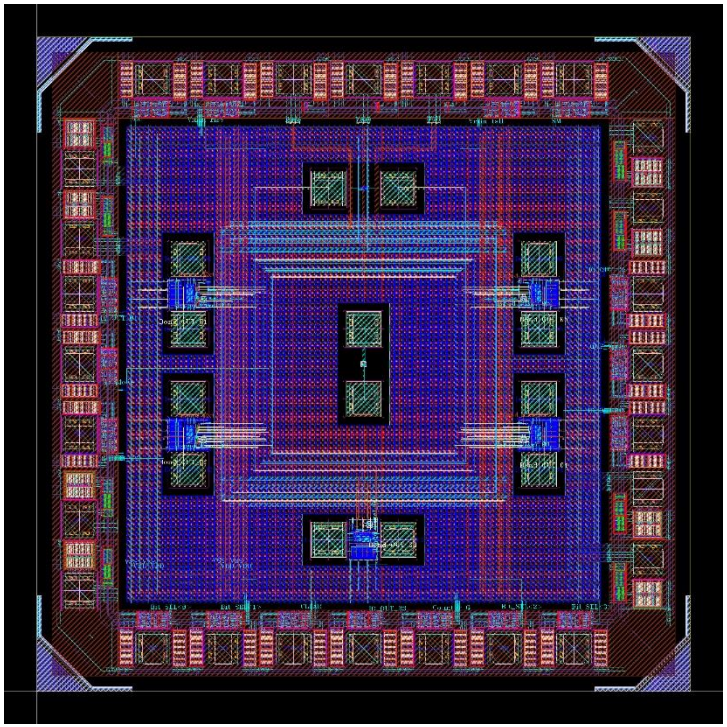


Pixel IO PAD Read-Out	**- SPAD Type #6** **- AFE Type #4**
Pixel Bond PAD Read-Out	- SPAD Type #36 - AFE Type #4
Only AFE Bond PAD Read-Out	- AFE Type #4
Only AFE IO PAD Read-Out	- AFE Type #4

	IO_PAD	Bond_PAD
Pixel (SPAD+AFE)	Pixel IO PAD Read-Out	Pixel Bond PAD Read-Out
Only AFE	Only AFE IO PAD Read-Out	Only AFE Bond PAD Read-Out

Achievements

- **Process** : DBH 110nm CIS (BSI)
- **Area** : 1,490um × 1,490um
- **Design** : SPAD AFEs & Device



<TOP View>

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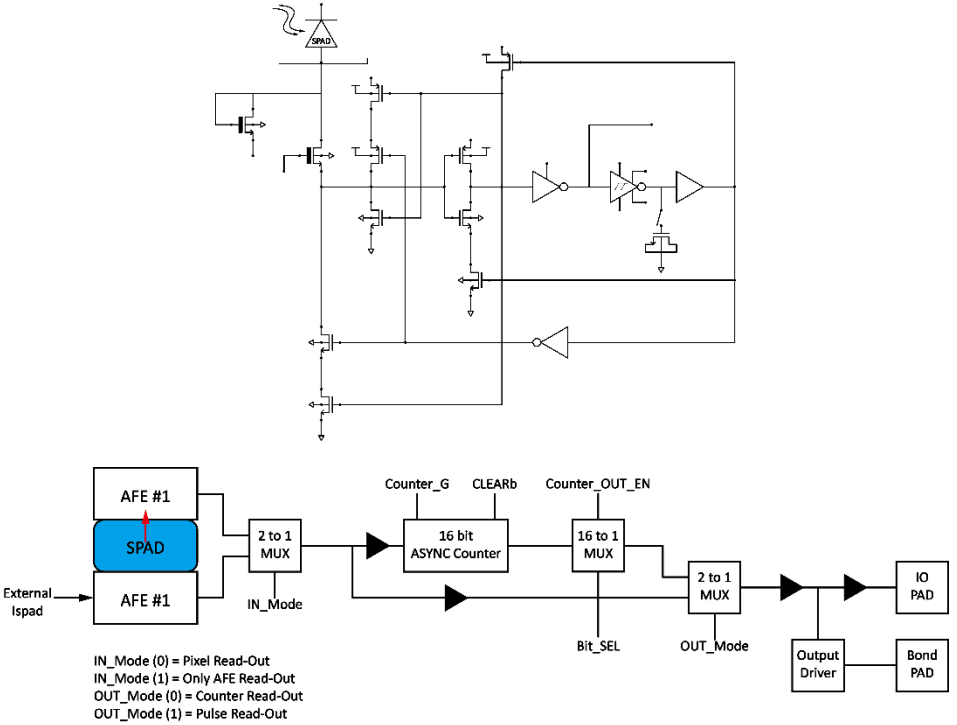
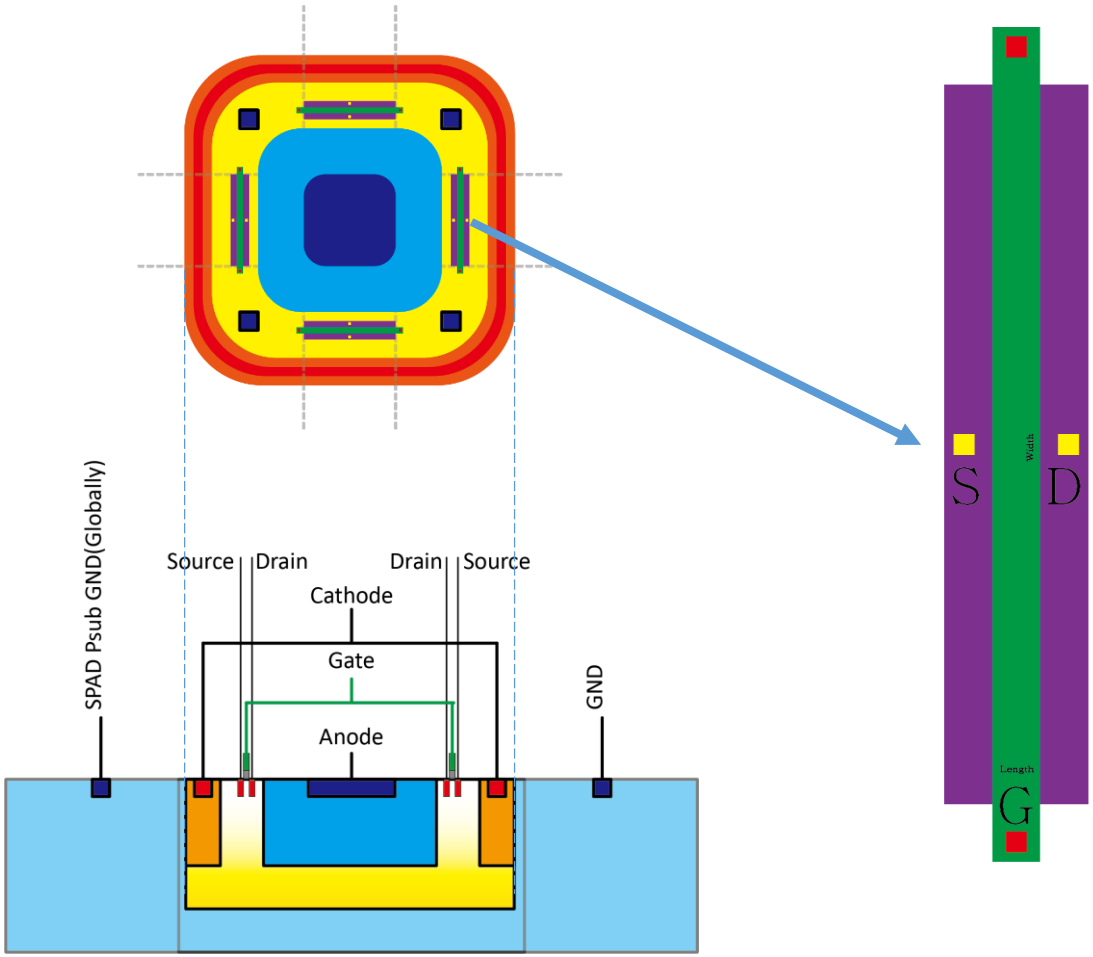


<SPAD AFE & Read-out>

Achievements

<SPAD Integrated with MOSFET>



Future Plan

1. Imaging System Setup (w/JH Kim)

2. SPAD Device Measurement & Thesis Writing

3. Research & Design Large SPAD Array using Verified AFE