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11th

RF INTEGRATED CIRCUIT TECHNOLOGY WORKSHOP

제11회 RF 집적회로 기술 워크샵

11th RF INTEGRATED CIRCUIT TECHNOLOGY WORKSHOP

- 일　　정 : 2011년 9월 22일 (목) ~ 24일 (토)
- 장　　소 : 제주시 라마다 프라자 호텔
- 주　　관 : 고려대학교 (BK21 정보기술 사업단)
  ETRI, 한국산업기술관리평가원, 지식경제부
- 주　　최 : 대한전자공학회 RF 집적회로기술연구회
- 공동주최 : 한국전자파학회(마이크로파 및 전파연구회),
  Seoul Chapter of IEEE SSCS, EDS, CAS,
  Korea Chapter of IEEE MTT, 동국대 밀리미터파신기술연구센터 (MINT),
  KAIST 지능형 RF 연구센터, KAIST 전파교육연구센터
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3-Gb/s Radio Link With SiGe BiCMOS 60-GHz Receiver Front-End

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Abstract

A 60-GHz receiver front-end consisting of a 60-GHz LNA, a 60-GHz down-mixer, and an output buffer is developed in 0.25-μm SiGe:C BiCMOS technology and demonstrated in 60-GHz radio link with a CMOS mixed-mode QPSK demodulator. We achieve 2-m wireless transmission of 3-Gb/s QPSK data with the bit error rate of 9×10^{-9}.

I. Introduction

Recently, 60-GHz wireless personal area networks (WPANs) have been strongly researched and silicon-based 60-GHz transceiver design and demonstration results have been reported. For example, C. Marcu *et al.* demonstrated 1-m wireless transmission of 4 Gb/s QPSK data utilizing the 60-GHz transceiver with integrated baseband circuitry in 90-nm CMOS technology [1].

The IEEE 802.15.3c standard for 60-GHz WPANs specifies three modes which are the single-carrier mode, the high-speed interface mode, and the audio/video mode for different target markets [2]. Among them, the single-carrier mode is designed for line-of-sight (LOS) operation and low-cost low-complexity applications such as mobile/kiosk applications. It provides data rate up to 5 Gb/s and less implementation complexity than other two modes based on OFDM.

We have previously developed a mixed-mode QPSK demodulator based on 1-bit resolution sampling for low-power low-complexity single-carrier 60-GHz WPANs [3]. 60-GHz radio link using the demodulator was successfully demonstrated with the data rate up to 3.4 Gb/s. In this paper, we develop a SiGe BiCMOS 60-GHz receiver front-end consisting of a 60-GHz LNA, a 60-GHz down-mixer, and an output buffer realized in IHP's 0.25-μm SiGe:C BiCMOS technology [4]. By utilizing the 60-GHz receiver and the QPSK demodulator, we demonstrate 2-m wireless transmission with 3-Gb/s QPSK data.

II. 60-GHz Receiver Front-End

The schematic of the 60-GHz LNA is shown in Figure 1 (a). The LNA is two-stage cascode design for high gain, low noise, and high isolation. The first and second stages are biased at optimized current density for minimum noise figure and maximum gain, respectively. For input matching of the first stage, simultaneous noise and input matching technique is used with tuning the transistor size, the emitter degeneration inductor, and the input capacitor and inductor [5]. The series inductors between the common-emitter and common-base transistors in each stage compensate the capacitances of two transistors and improve the gain performance [6]. The LNA dissipates the total current of 7 mA from the supply voltage of 2.5 V where the first and second stages consume 2.8 mA and 4.2 mA, respectively.

Figure 1 (b) shows the schematic of the 60-GHz down-mixer including the output buffer. The singly-balanced mixer topology was chosen to use single-ended LNA output directly without a lossy and large-size transformer for single-to-differential conversion. Emitter degeneration at the transconductance transistor improves the linearity with sacrificing the conversion gain. The LO signal is differentially applied to the mixer with the power of 6 dBm. The resistive load was used for wide IF bandwidth and carefully optimized between the conversion gain and the IF bandwidth. Emitter followers were used for high-linear output buffers, and the output impedance was matched to 50 Ω. The mixer core and the output buffer dissipate 5.2 mA and 4.7 mA from the supply voltage of 2.5 V, respectively.

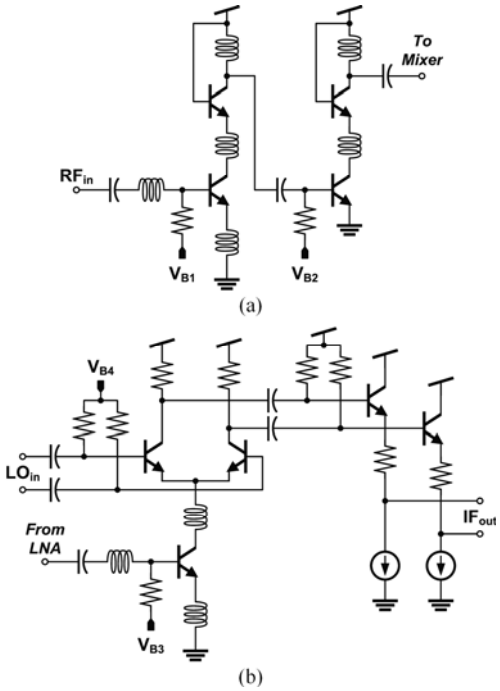

Figure 1. Schematics of (a) 60-GHz LNA and (b) 60-GHz down-mixer

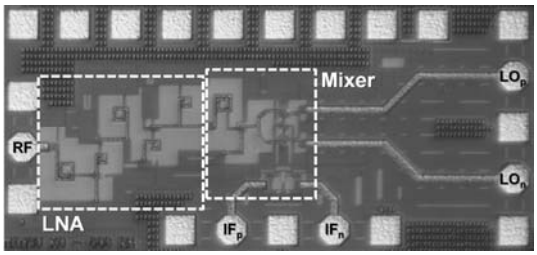

Figure 2. Chip photo of 60-GHz receiver front-end

The chip photo of the fabricated 60-Ghz receiver front-end is shown in Figure 2. The single-ended RF is connected to a 100-μm-pitch ground-signal-ground (GSG) probe, and the differential LO and IF are connected to GSGSG probes. The chip area including all pads is 1040 μm × 470 μm.

Measured performance of the 60-GHz receiver front-end is shown in Figure 3. Figure 3 (a) shows the measured conversion gain at different RF frequencies while the IF frequency was fixed at 4 GHz. The conversion gain over 10 dB is obtained in the RF frequency range of 58 to 66 GHz. The peak conversion gain is 16 dB at 62 GHz. Figure 3 (b) shows the measured conversion gain at different IF frequencies while the LO frequency was fixed at 58 GHz. The 3-dB IF bandwidth of about 6 GHz is obtained.

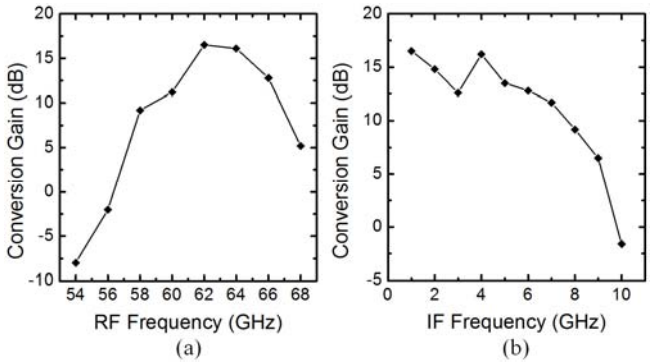

Figure 3. Measured conversion gain of 60-GHz receiver front-end at (a) different RF frequencies (fixed IF frequency of 4 GHz) and (b) different IF frequencies (fixed LO frequency of 58 GHz)

III. 3-Gb/s Radio Link Demonstration

3-Gb/s QPSK data transmission via 60-GHz radio link was demonstrated using the developed 60-GHz receiver front-end. Figure 4 shows the experimental setup. Link components except for the 60-GHz receiver and the QPSK demodulator are commercial external devices. In the transmitter, A QPSK modulator converts 2^7-1 PRBS data from a pattern generator into QPSK data with the carrier frequency of 4.8 GHz. A 60-GHz transmitter front-end consisting of a LO, an up-mixer, a bandpass filter, and a power amplifier frequency up-converts and amplifies the desired signal. The LO frequency of 56.7 GHz was chosen because the optimum center frequency of the 3-Gb/s QPSK signal is 61.5 GHz for the best link performance. The transmitter output signal has the power of -1 dBm, and its spectrum is shown in Figure 5 (a). The signal is transmitted to the receiver using 24-dBi horn antennas for LOS operation. The wireless distance is 2 m, and channel loss including cable loss is 32.5 dB. The 60-GHz receiver front-end frequency down-converts the 60-GHz-band signal into the IF signal with another 56.7-GHz LO. The QPSK demodulator converts the IF signal into baseband data in I and Q channels. An IF amplifier is used to satisfy the input sensitivity of the QPSK demodulator.

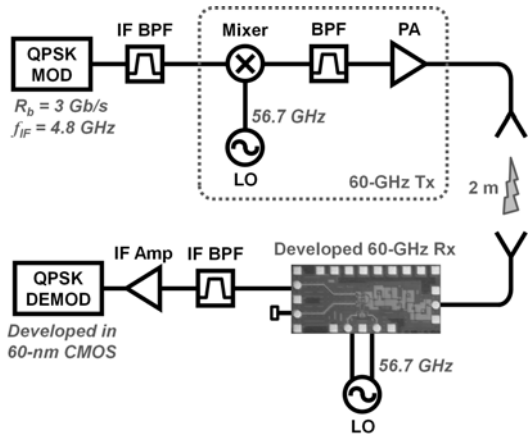

Figure 4. Experimental setup for 60-GHz radio link demonstration

Demodulated data at the demodulator output were analyzed in terms of BER and eye diagram using a BER tester. The minimum BER of 9×10^{-9} was measured for the I channel when the 60-GHz receiver input power was -33.5 dBm. BER performance is limited by unflat gain response of the 60-GHz receiver as shown in Figure 3 (a) and the VCO of the demodulator [3]. The measured eye diagram at this point is shown in Figure 5 (b). Thick transition lines are due to the quantized timing error of the demodulator [3].

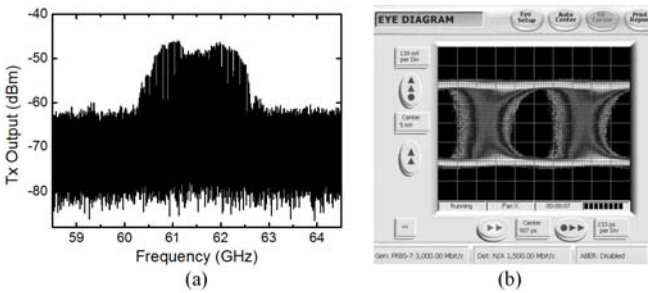

Figure 5. Demonstration results of 3-Gb/s QPSK data transmission in 60-GHz radio link; (a) Spectrum of transmitter output signal and (b) eye diagram of I channel of demodulated data

IV. Conclusion

60-GHz radio link is successfully demonstrated using the SiGe BiCMOS 60-GHz receiver front-end and the CMOS 3-Gb/s mixed-mode QPSK demodulator. It shows that our scheme can be used for low-cost single-carrier 60-GHz WPAN applications.

Acknowledgements

The authors thank IDEC for EDA software support.

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