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60-GHz Voltage-Controlled Oscillator and Frequency Divider in 0.25- μm SiGe BiCMOS Technology

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Abstract— We present an integrated 60-GHz voltage-controlled oscillator (VCO) and frequency divider (FD) chain in a 0.25- μm SiGe BiCMOS technology. To achieve the wide tuning range, the VCO employs a differential Colpitts configuration and the FD is a regenerative type based on Gilbert-cell mixer and bandpass filter. The VCO-FD chain achieves the tuning range from 54 to 63 GHz and the phase noise of -96.5 dBc/Hz at 1-MHz offset. The power consumption is 46 mW with supply voltage of 3.3 V excluding output buffers.

Keywords— Colpitts voltage-controlled oscillator (VCO), SiGe BiCMOS, regenerative frequency divider (FD), wide tuning

I. INTRODUCTION

Silicon-based 60-GHz transceivers have been extensively researched for wireless personal area network and wireless local area network applications. For these applications, the transceiver should operate in the wide frequency range in order to cover the 9-GHz unlicensed band around 60 GHz. For such transceivers, phase-locked loops (PLLs) having a wide tuning range is essential [1]. The traditional way of realizing voltage-controlled oscillators (VCOs) for such PLLs is using push-push VCOs or VCOs with differentially shielded inductors. Push-push VCOs employ a complicated structure with many varactor banks for coarse and fine tuning [2]. In addition, they suffer from large DC power dissipation and low output power [3] due to the second harmonic component. VCOs with differential shielded inductors do not provide a sufficient tuning range and have low output power.

Frequency dividers (FDs) are widely used for frequency synthesizers and the key design criteria are wide tuning range, low input power and minimum power consumption. For a wide locking range, the flip-flop-based static divider is used. However, it suffers from high power consumption and limited operation frequencies. The injection-locked frequency divider (ILFD) has the highest operation frequency while providing the narrowest locking range [4]. At a high operation frequency, regenerative divider has a wide frequency tuning range than ILFD and low power consumption than static divider.

In this paper, we report a 60-GHz differential Colpitts VCO which has a wide tuning range, large output power, and low phase noise. In addition, the VCO is integrated with a wide tuning range regenerative frequency divider. The integrated VCO-divider chain is realized in 0.25- μm SiGe BiCMOS Technology.

II. CIRCUIT DESCRIPTION

A. Balanced Colpitts VCO

The circuit schematic of the proposed VCO is shown in Fig. 1. Common collector and balanced Colpitts VCO are implemented with improvement in phase noise. The VCO is composed of core which has capacitive divider (C_T , C_{VAR}), tank inductor (L_T), output buffer (Q_5 , Q_6 , L_{Buf}) and tail current source (Q_1 , Q_2). Oscillation frequency is determined by loop

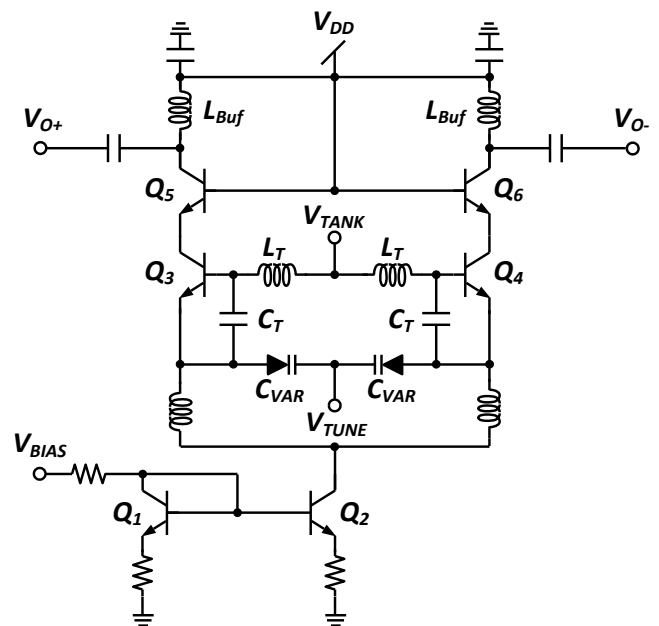


Figure 1. Schematic diagram of 60-GHz balanced Colpitts VCO.

gain to satisfy the Barkhausen criterion [5] for oscillation. This loop gain must exceed unity gain to oscillate. Oscillation frequency is decided by composition of C_T , C_{VAR} and L_T .

B. Regenerative Frequency Divider

The regenerative frequency divider is based on a double balanced Gilbert-cell mixer with inductive load as shown in Fig. 2. The output node of Gilbert-cell mixer is fed back to the gates of trans-conductance transistors (Q_2 , Q_3). The input signal at w_{in} is mixed with feedback signal at $w_{in}/2$ then mixed sideband signals exist at $w_{in}/2$ and $3w_{in}/2$. The bandpass filter selects lower sideband and it survives and circulates around the loop. [6] Load inductors L_P resonate with parasitic capacitances at output node. These capacitances are consisting of drain capacitances of switching transistors (Q_4 - Q_7), input gate capacitances of trans-conductance transistors (Q_2 , Q_3) and output buffer transistors. To obtain closed loop gain over unity, the mixer should have conversion gain over unity and 180° phase difference between output and input nodes.

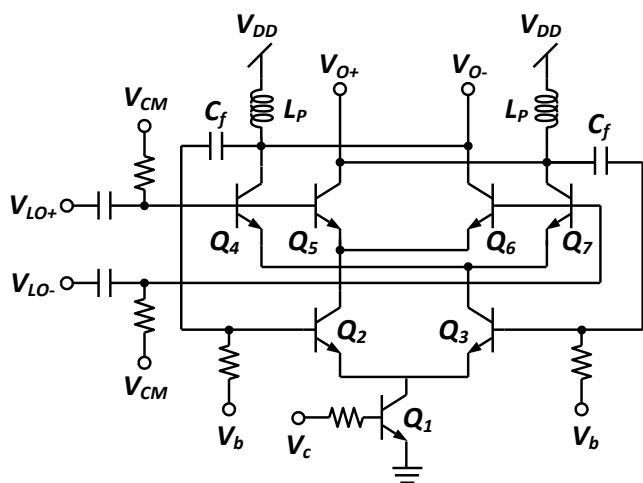


Figure 2. Schematic diagram of 60-GHz regenerative divider.

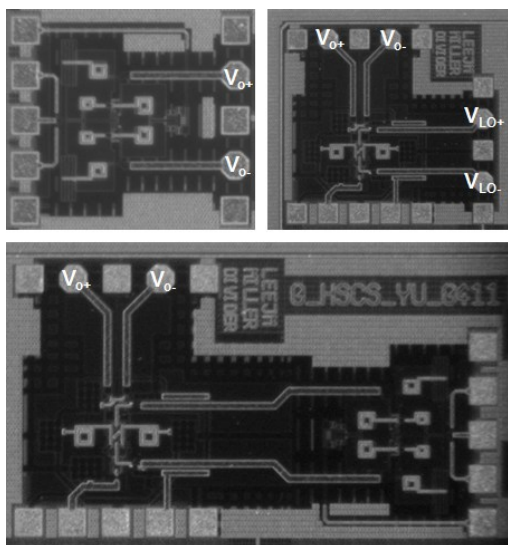


Figure 3. Photographs of VCO, regenerative frequency divider and integrated VCO-divider chain.

III. MEASUREMENT RESULTS AND DISCUSSION

VCO and regenerative frequency divider are fabricated in IHP 0.25- μm SiGe BiCMOS SG25H3 process [7]. The process offers 6 metal layers for interconnect, MIM capacitors of $2 \text{ fF}/\mu\text{m}^2$, and f_T and f_{max} of 110 GHz and 180 GHz. Die photos of VCO, FD and integrated VCO-divider chain are shown in Fig. 3. Each chip area including pads are about $460 \times 530 \mu\text{m}^2$, $610 \times 650 \mu\text{m}^2$ and $1100 \times 610 \mu\text{m}^2$. They are measured on wafer probing. Fig. 4 shows measured output tuning characteristics of VCO. By varying V_{TUNE} , oscillation frequency of VCO is tuned between 50 to 67.4 GHz with a 28.3% tuning range. The output power is varied from -4 to 0.67 dBm. The VCO consumes 32 mW with supply voltage of 3.2 V including output buffers. Fig. 5 shows input sensitivity and bandwidth of the FD. A minimum input power of 1.33 dBm is required at 62 GHz and frequency range is from 52 GHz to 67 GHz with a 25.2% tuning range. The FD consumes 14.39 mW with supply voltage of 3.3 V excluding output buffers. Fig. 6 shows the measured output tuning characteristics of VCO and integrated VCO-divider chain. The output power of the VCO is larger than sensitivity of the FD, because input matching is not established in this FD design. The output power of VCO is lower than sensitivity in the integrated VCO-divider chain. Then, this chain could tune between 54 to 63 GHz with 15.4% tuning range. The integrated VCO-divider chain consumes 46 mW excluding output buffers of the FD. Fig. 7 shows the measured

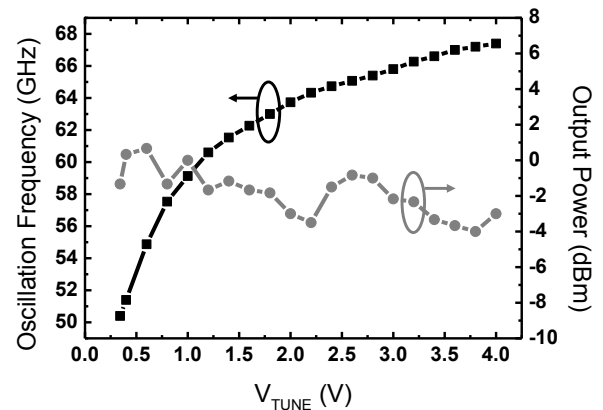


Figure 4. Measured oscillation frequency and output power versus tuning voltage of the VCO.

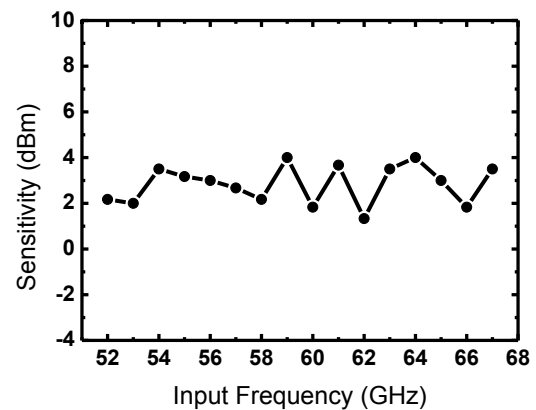


Figure 5. Input sensitivity of regenerative frequency divider.

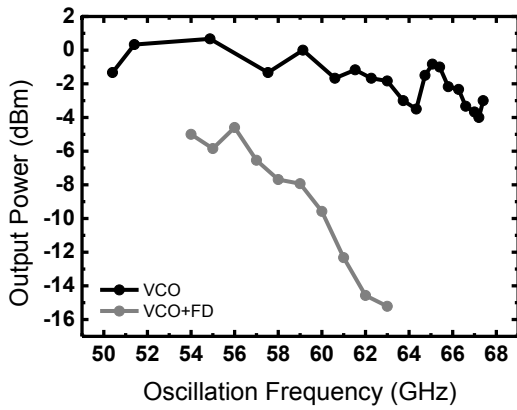


Figure 6. Measured maximum output power versus oscillation frequency of VCO and integrated VCO-divider chain.

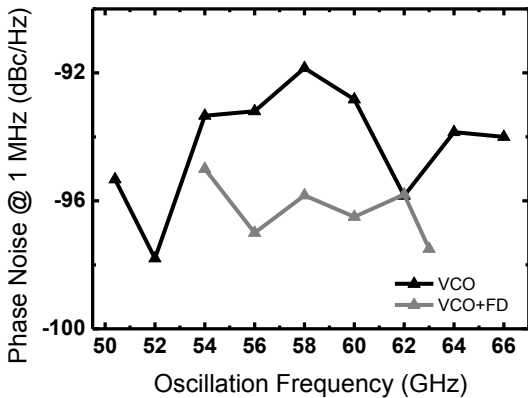


Figure 7. Measured phase noise at 1-MHz offset versus oscillation frequency of the VCO and integrated VCO-divider chain.

phase noise at 1-MHz offset versus oscillation frequency. This integrated VCO-divider chain has less than ± 2 dB phase noise variation from -97 to -95 dBc/Hz. This phase noise is lower than that of VCO. Finally, the output spectrum of the integrated VCO-divider chain at a 30 GHz is shown in Fig. 8. The spectrum shows a measured maximum deembedded output power, and embedded power is -9.6 dBm at an output frequency of 30 GHz.

IV. CONCLUSION

In this paper, we realized a wide tuning range 60-GHz VCO, regenerative frequency divider, and the integrated VCO-divider chain in a 0.25- μm SiGe BiCMOS process. VCO has 17.4-GHz bandwidth with 28.3% tuning range. Regenerative frequency divider has 15-GHz bandwidth with 25.2% tuning range and minimum input sensitivity is 1.33 dBm at 62 GHz.

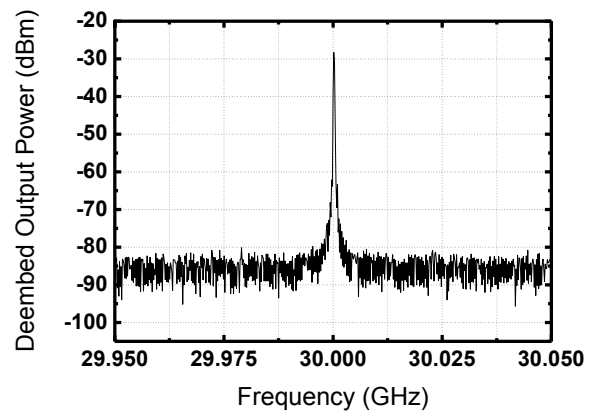


Figure 8. Deembedded output spectrum of the integrated VCO-divider chain at a divided frequency, 30 GHz, with a frequency span of 100 MHz (RBW = 100 kHz, VBW = 10 kHz).

The integrated VCO-divider chain achieves 9-GHz bandwidth with 15.4 % tuning range and consumes 46 mW excluding output buffer of the FD. The phase noise varies from -97 to -95 dBc/Hz at 1-MHz offset. The realized circuits can be used for 60-GHz phase-locked loops having a wide tuning range.

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