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Tuesday, November 6, 2012

Session 5

Analog and Mixed-Signal Circuits - 1

08:30~10:00 Regular Session 5 Ramada-1

Chair Karsten Leitis (Univ. of Applied Sciences Giessen-Friedberg, Germany)

- [RS5-1] Current Equalization Scheme For Parallel Low-Dropout Regulators**
 Siddharth Katare and Narayanan Natarajan
 Intel Technology India, India 88
- [RS5-2] A CMOS Voltage Reference Combining Body Effect with Switched-Current Technique**
 Ning REN, Hao ZHANG and Tsutomu YOSHIHARA
 Waseda University, Japan 92
- [RS5-3] Design and Analysis of a Power-Efficient Cascode-Compensated Amplifier**
 Shafqat Ali, Steve Tanner and Pierre-André Farine
 Swiss Federal Institute of Technology (EPFL), Switzerland 96
- [RS5-4] Spur Suppression in Frequency Synthesizer using Switched Capacitor Array**
 Debashis Mandal, Student Member, IEEE, Pradip Mandal, Member, IEEE, and Tarun Kanti
 Bhattacharyya
 Indian Institute of Technology, India 100

Session 6

Analog and Mixed-Signal Circuits - 2

13:30~15:00 Regular Session 6 Ramada-2

Chair Hung-Wen Lin (YuanZe University, Taiwan)

- [RS6-1] A 10-Gb/s Power and Area Efficient Clock and Data Recovery Circuit in 65-nm CMOS Technology**
 Jinsoo Rhim, Kwang-Chun Choi and Woo-Young Choi
 Yonsei University, Korea 104
- [RS6-2] A Digitally Enhanced Low-Distortion Delta-Sigma Modulator for Wideband Application**
 Jae-Hyeon Shin, Kang-Il Cho, Gil-Cho Ahn
 Sogang University, Korea 108
- [RS6-3] Digitizing the Feedback Signal in a Magnetic Field (AMR) Sensor System Using Delta Sigma Modulator Topology**
 Tommy Halim, Karsten Leitis
 University of Applied Sciences Giessen-Friedberg Friedberg, Germany 112
- [RS6-4] A DLL-Based FSK Demodulator for 5.8GHz DSRC/ETC RF Receiver**
 Hung-Wen Lin, Hsin-Lin Hu, Wu-Wei Lin
 YuanZe University, Taiwan 116

A 10-Gb/s Power and Area Efficient Clock and Data Recovery Circuit in 65-nm CMOS Technology

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Abstract—This paper reports a 10-Gb/s power and area efficient clock and data recovery circuit implemented in 65-nm CMOS technology. CMOS static circuits are used as much as possible so that the power consumption and the chip area can be minimized. In order to alleviate the supply sensitivity of CMOS static circuits, a supply-regulator is implemented. At 10-Gb/s, the clock and data recovery circuit consumes 5-mW of power and occupies 0.0075mm² of area.

Keywords—component; Clock and data recovery; power and area efficient; CMOS static circuits; 65-nm CMOS technology

I. INTRODUCTION

Power and area efficiency are important requirements in many high-speed interface circuits. Along with the growing demand for single-chip integration of various function blocks, the power and area constraints are becoming very tight. For example, Fukuda *et al.* reported a transceiver that has 0.98-mW/Gb/s power efficiency and chip area of 0.48-mm² [1].

Many research efforts are needed to provide solutions that are power and area efficient. Using CMOS static circuit is one possible solution since they are power and area efficient compared to differential circuits. CMOS static circuits only consume dynamic power while differential circuits consume static power as well. They also allow smaller size devices resulting in area reduction. Recent development in CMOS technology allows CMOS static circuits for high-speed interface applications [2].

In this paper, we report a 10-Gb/s Clock and Data Recovery (CDR) circuit implemented in 65-nm CMOS technology. We used CMOS static circuit as much as possible to maximize power and area efficiency.

II. CDR ARCHITECTURE

Since CMOS static circuits are more vulnerable to noises, such as power supply noise, supply regulation is essential for the system having CMOS static circuits. Fig. 1 shows the overall block diagram of our CDR. It is a conventional PLL-

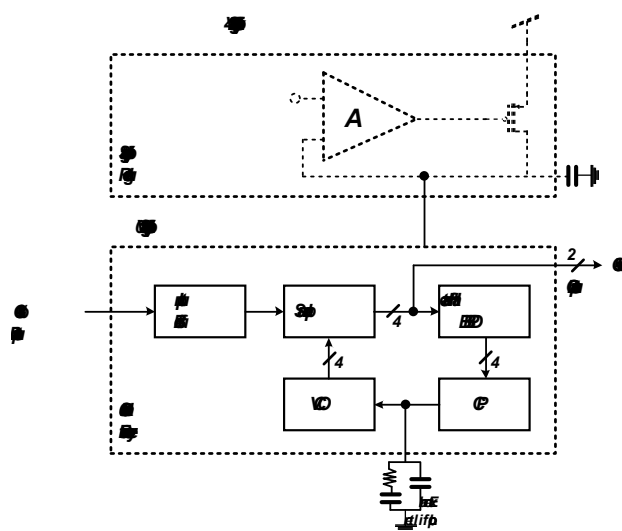


Fig. 1. Overall block diagram of CDR circuit

based CDR with a supply regulator which generates internal supply voltage required for CDR core from the external supply voltage. The capacitor required for the stability of regulator is externally implemented.

The CDR circuit is designed using the half-rate topology in order to reduce the speed burden. The Voltage Controlled Oscillator (VCO) provides four phases of 5-GHz clock to the sampler. The half-rate Bang-Bang type Phase Detector (BBPD) compares four samples and generates up/down pulses which are integrated by the charge pump. The loop-filter of the CDR is externally implemented.

III. CIRCUIT DESCRIPTION

A. Voltage Controlled Oscillator

Our VCO is based on modified Lee & Kim delay-cell which has good power efficiency and phase noise characteristics as well as wide tuning-range [3]. As shown in fig. 2, the VCO in our design is a two-stage ring-type oscillator. Two-stage is sufficient for oscillation since Lee &

Kim delay-cell is a feed-forward structure [4]. The coarse and fine control nodes are used for frequency and phase acquisition, respectively.

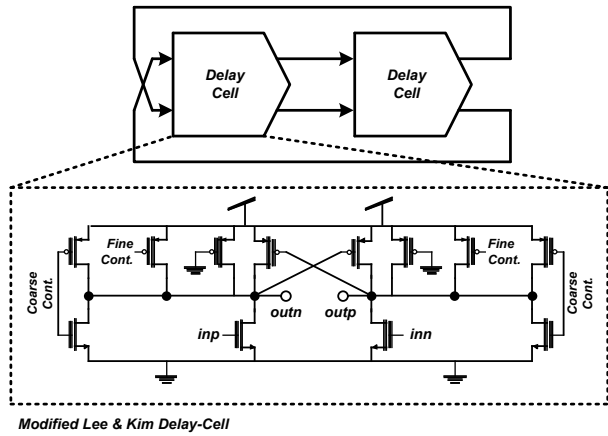


Fig. 2. Schematic of VCO and modified Lee & Kim delay-cell

B. Sampler & Half-rate BBPD

A sense-amplifier-based flip-flop (SAFFs) consumes less power and occupies smaller area compared to other differential logics such as CML [5]. Using SAFF as a sampler, additional level conversion circuits are not needed since the sense-amplifier generates rail-to-rail output. This reduces additional power and area.

As shown in fig. 3, half-rate BBPD is composed of four exclusive-OR (XOR) gates which compare two consecutive sampler outputs and generate up/down pulses. The up/down pulses are generated only when there is a transition, which prevents dithering of the output with long-run patterns [6].

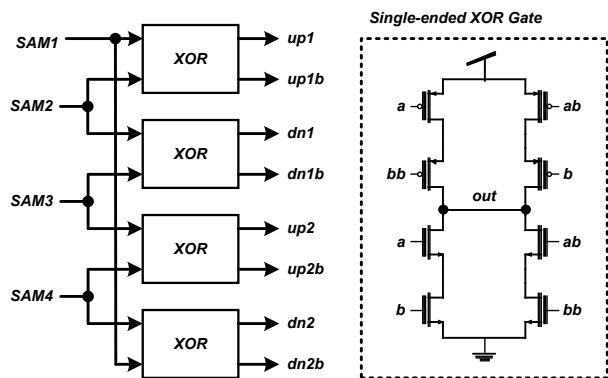


Fig. 3. Bang-bang type phase detector and schematic of exclusive-OR gate

C. Charge Pump & Supply Regulator

The switches in the charge pump turn on/off complementarily as shown in fig. 4. This structure reduces output voltage glitches and enables faster switching as only the current path is changed. The bias voltages are provided from the replica feedback circuit.

A two-stage amplifier is designed for the replica feedback. The first stage amplifier has a folded-cascode structure so that it can take rail-to-rail input. The second stage provides high gain and small bandwidth, which ensures the phase margin of the feedback loop. The schematic of the amplifier is shown in fig. 5.

The supply regulator is composed of an amplifier having the same structure as the one used in charge pump, and a power PMOS. The size of the PMOS is sufficiently large so that it can take the total current required for the CDR.

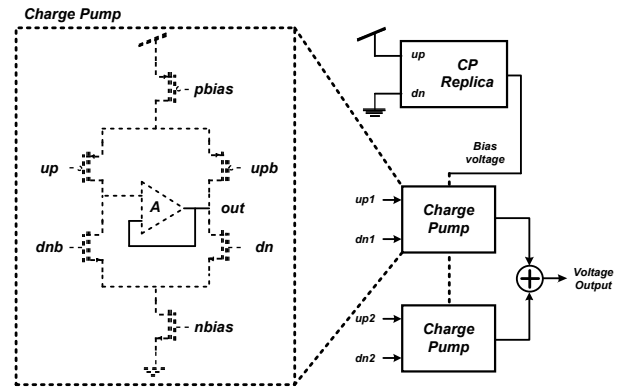


Fig. 4. Schematic of the complementary charge pump

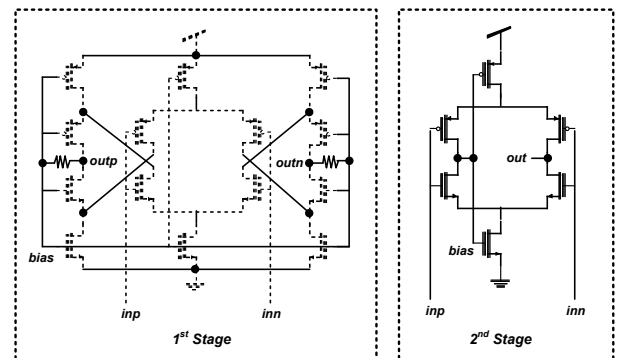


Fig. 5. Schematic of two-stage amplifier of the charge pump and supply regulator

IV. MEASUREMENTS

A prototype chip is implemented with standard 65-nm CMOS technology. Fig. 6 shows the microphotograph of the fabricated chip. Our CDR core occupies 75- μm x 100- μm of area and consumes 5-mW of power with 1.4-V supply voltage. 10-Gb/s PRBS-7 pattern data having amplitude of 400-mV were introduced to the chip on a probe station. The recovered clock and data were observed with a spectrum analyzer and a BER tester with a built-in oscilloscope, respectively. Fig. 7 shows the measurement setup.

The power spectrum of the recovered clock is shown in fig. 8(a). The measured phase noise at 1-MHz offset is -101.3-dBc/Hz as shown in fig. 8(b). The oscilloscope output of the

recovered clock is shown in fig. 9 (a). The peak-to-peak jitter and the RMS jitter of the recovered clock are 42-ps and 7-ps respectively. The eye-diagram of the recovered data is shown in fig. 9 (b). No error has been monitored for more than 200-seconds and achieved BER less than 10^{-12} .

The performance summary of our CDR and comparison with other papers are provided in table 1. The Figure Of Merit (FOM) is defined as the following equation.

$$FOM = \frac{\text{Power Consumption [mW]}}{\text{Data-rate [Gb/s]}} \times \frac{\text{Area [mm}^2\text{]}}{\left(\frac{\text{Technology [nm]}}{65}\right)^2} \quad (1)$$

The FOM consists of power-consumption, data-rate, area and the technology. The area is normalized to the technology and the power consumption is normalized to the data-rate [7]. The active area of the chip is considered in this comparison. Our CDR shows the best FOM performance since it occupies the least area while it consumes compatible amount of power at given data-rate.

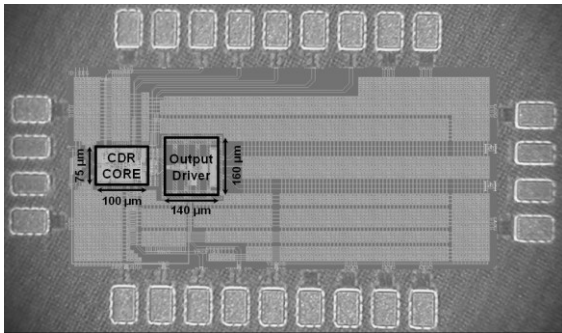


Fig. 6. Microphotograph of the fabricated chip

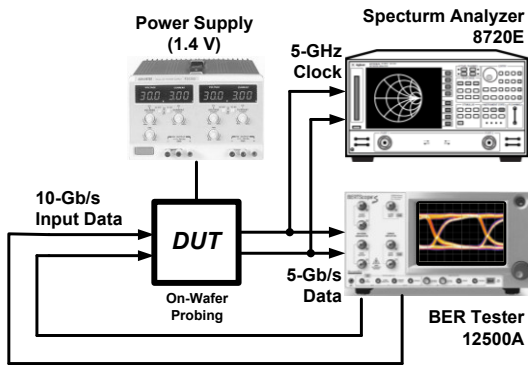
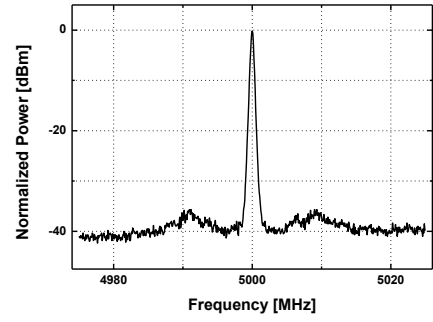
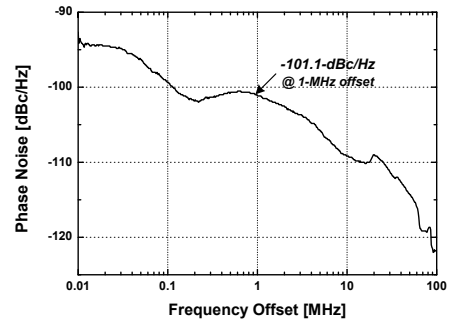


Fig. 7. Setup for the measurements

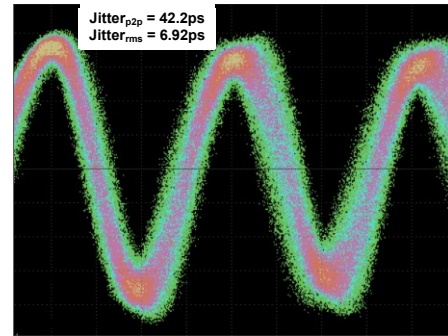


(a)

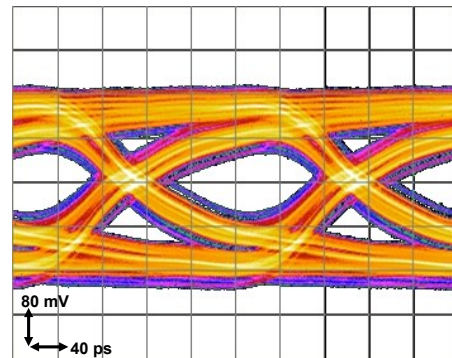


(b)

Fig. 8. (a) Power spectrum and (b) phase noise characteristics of the recovered clock



(a)



(b)

Fig. 9. Eye-diagram of the (a) recovered clock and (b) recovered data

TABLE I. PERFORMANCE SUMMARY AND COMPARISONS (MEASUREMENTS)

	[8]	[9]	[10]	[11]	[1]	This work
Technology [nm]	180	180	90	65	65	65
Power Supply [V]	1.4	1.8	1.2	1	1	1.4
Data-rate [Gb/s]	0.2-4	5	6.4-7.2	1-6	12.5	10
BER	$< 10^{-12}$	$< 10^{-12}$	$< 10^{-12}$	N/A	$< 10^{-12}$	$< 10^{-12}$
Jitter [ps]	28	57.4	N/A	N/A	8.5	42
Power Consumption [mw]	14	144	3.74	22	5	5
Area (active) [mm ²]	0.8	0.66	0.0139 (estimated)	0.018	0.024 (estimated)	0.0075
Power Efficiency [mW/Gb/s]	7	28.8	0.6	3.7	0.4	0.5
FOM	0.73025	2.47867	0.00434	0.066	0.0096	0.00375

V. CONCLUSION

This paper focuses on power reduction of the CDR circuit. CMOS static circuits are fully utilized for our design and we achieved 5-mW of power consumption at 10-Gb/s data-rate. In order to reduce the supply sensitivity of the CMOS static circuits, supply regulator is also designed. The operation of the 10-Gb/s CDR circuit has been successfully verified with the fabricated chip. When compared to previous works, our CDR shows the best FOM performance.

ACKNOWLEDGMENT

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