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SITEMAP
제22회 한국반도체학술대회
The 22nd Korean Conference on Semiconductors
대회개요
프로그램
초록제출
논문발표
참가등록
전시/후원
숙박예약
장소안내
커뮤니티
- 숙박안내
- 온라인 예약
제22회 한국반도체학술대회 2015년 2월 10일(화)~12일(목)
The 22nd Korean Conference on Semiconductors 인천 송도컨벤시아
Breakthrough the Limitations of Semiconductor Technology (More Moore & More than Moore)
제22회 한국반도체학술대회가 성황리에 개최되었습니다.
2016년 2월 제23회 한국반도체학술대회도 많은 관심과 성원 부탁 드리겠습니다.
초록집 다운로드
모든 사진 다운로드
게재 학술지 안내
Short Course
구두발표
포스터발표
기조강연
반도체인의 밤
Chip Design Contest
행사장
KCS 2015
February 10~12
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논문작성양식
논문제출
초록접수마감
2014.11.30(일)
2014.10.31(금)
사전등록
숙박예약
초록채택통보
2014.12.29(월)
2014.12.15(금)
Call for Paper
프로그램
사전등록마감
2015.01.30(금)
공지사항 | KCS 2015에 대한 최근 소식을 알려드립니다.
최종발표일정이 안내되었습니다.
초록채택통보가 안내되었습니다!
"제17회 한국 MEMS 학술대회" CFP를 확인하세요!
온라인 초록접수 프로그램이 오픈되었습니다.
주관
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3월 20일
한국반도체학술대회 현재 KCS 2016 준비중에 있습니다
AA
4월 말, KCS 2016 일정과 장소에 대해 SNS를 통해 먼저 공지를 할 예정이오니, 많은 관심 부탁 드립니다!!
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KCS @KCS_2015 10 Feb
제22회 한국반도체학술대회가 오늘 10일 Short Course를 시작으로 개최됩니다. 다양한 프로그램이 준비되었사오니, 반도체인들의 많은 참석과 관심 부탁 드립니다. :)
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KCS @KCS_2015 31 Dec
2014년의 마지막날 입니다. 다사다난했던 2014년 모두 고생 많으셨습니다. 2015년 새해 이루고자 하시는 일들 모두 성취하시는 한 해가 되기를 바랍니다.
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M. RF Design 분과

Room K
1F / 102+103호

2015년 2월 12일(목) 13:10-14:40
[TK2-M] CMOS RF Device and Circuit Solutions
좌장: 이강윤 (성균관대학교), 박준배 (아나패스)

TK2-M-1	**13:10-13:25**	**Circuit-Level Modeling of 10-Gbps Si-Photonic Transceiver** Minkyu Kim, Myungjin Shin, Tongsung Kim, and Woo-Young Choi Department of Electrical and Electronic Engineering, Yonsei University
TK2-M-2	**13:25-13:40**	**The Conducted Radiation Modeling Method for Automotive IC** Sanghyeon Park, Dongsoo Lee, and Kang-Yoon Lee Department of Information and Communication Engeeneering, SungKyunKwan University
TK2-M-3	**13:40-13:55**	**Performance Improvement of On-Chip Inductor Using Novel Patterned Ground Shield Structure and Thick Metal Layer** Jin-Woong Jeong, Sung-Yong Jang, Sung-Woo Lee, Sung-Kyu Kwon, Choul-Young Kim, Ga-Won Lee, and Hi-Deok Lee Dept. of Electronics Engineering, Chungnam National University
TK2-M-4	**13:55-14:10**	**Low Power, Wide Range, High Speed Digitally Controlled Ring Oscillator** Seong Jin Oh, Sang-Yoon Kim, and Kang-Yoon Lee College of Information and Communication Engineering, Sungkyunkwan University
TK2-M-5	**14:10-14:25**	**10bit Low Power SAR ADC Design for Multi-Channel Sensing** Dong-Hyeon Seo, Hyung-Gu Park, and Kang-Yoon Lee Information and Communication Engineering, Sungkyunkwan University
TK2-M-6	**14:25-14:40**	**A Third Order Active Notch Filter with Process Variation Compensation and Tunable Frequency Range for Suppressing Spurious Emission** Seung-Won Choi, Dong-Soo Lee, and Kang-Yoon Lee College on Information and Communication Engineering, SungKyunKwan University

Circuit-Level Modeling of 10-Gbps Si-Photonic Transceiver

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Recently, there are growing interests in Si-photonics for optical interconnect applications as it can provide high-performance integrated photonic devices in a cost-effective manner [1]. For successful design of integrated Si-photonic and electronic circuits for the target interconnect applications, it is very important to co-simulate photonic devices and electonic circuits on a single simulation platform. In this paper, we present a behaviour model of Si micro-ring modulator implemented in Verilog-A, a hardware description language often used for high-level behavioral modeling of electronic systems, and circuit-level simulation of this behaviour model with other electronic circuits for 10-Gbps transceiver realization. Fig. 1(a) shows the block diagram for the target transceiver. The electronic circuit block is composed of PRBS generator and error-rate tester that allow on-chip self-testing, for serializer and deserializer, modulator driver and transimpedance amplifier. The optical block consists of Si micro-ring resonator and Ge photodetector. Fig. 1(b) and (c) are trasmitted and received eye diagrams, respectively, obained from the simulation done entirely in Spice. With such co-simulation of photonic devices and electronic circuits, design optimization of the entire Si-photonic transceiver can be easily performed allowing more successful implementation of the target optical interconnects in a more cost-effective manner.

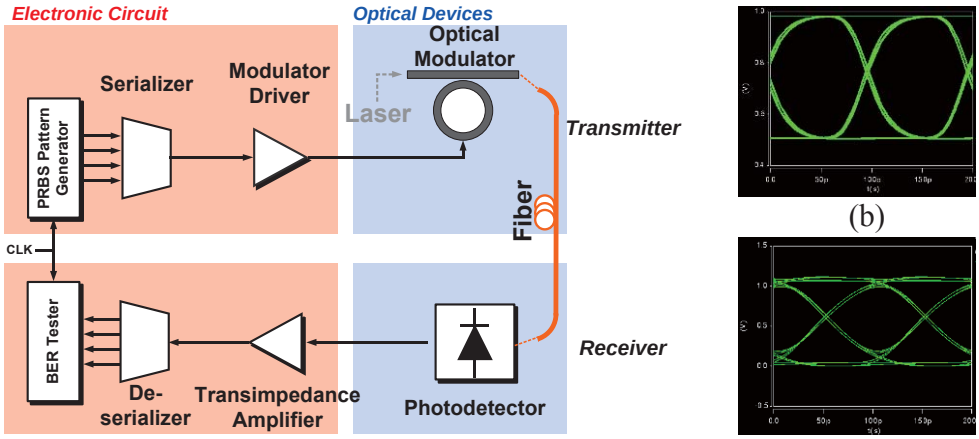

Fig 1. (a) Block diagram of Si-photonic transceiver and eye-diagram of (b) transmitted data and (c) received data

[1] X. Zheng *et al.*, Optics Express(2011), Vol. 19, No. 6