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IEEE Asian Solid-State Circuits Conference

- Home
- Organization
- Call for Papers & Participants
- Program
- Speakers Rehearsal
- Registration
- Hotel Reservation
- VISA Application
- Student Travel Grant Award
- Sponsorship
- Supporter and Exhibition
- Venue & Access
- General Information

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- Early bird registration is now available
- The notification of paper selection result has been distributed to all authors. In case that the authors have not received the notification, contact a-sscc2016@semiconportal.com
- Advanced Technical Program for A-SSCC 2016 is available.
- A-SSCC 2016 paper submission is closed. The acceptance notification is scheduled on August 5(EST).

A-SSCC2016

IEEE Asian Solid-State Circuits Conference
Toyama International Conference Center
Toyama, Japan

The IEEE A-SSCC (Asian Solid-State Circuits Conference) is an international forum for

Wednesday Nov 9th, 2016	8:30	Registration opens						
	09:00-09:45 (45min)	Session 10 PLENARY SPEECH Ⅲ					Supporters' Exhibition	
	09:45-10:30 (45min)	Session 11 PLENARY SPEECH Ⅳ						
	10:30-10:50 (20min)	Break(Drinks & Refreshments)						
	10:50-12:55 (125min)		Session 12 EFFICIENCY AND RELIABILITY ENHANCEMENT IN DIGITAL SYSTEMS Chr: Jun Zhou Track: DCS	Session 13 NYQUIST ADCS Chr: Takeshi Yoshida Track: DC	Session 14 MEMORY Chr: Atsushi Kawasumi Track: MEM	Session 15 BIOMEDICAL CIRCUITS AND SYSTEMS Chr: Noriyuki Miura Track: ETA		
	12:55-14:20 (85min)	Lunch Break						
	14:20-16:00 (100nin)		Session 16 DC-DC CONVERTER Chr: Nobukazu Takai Track: ACS	Session 17 WIRELINE TRANSMITTER TECHNIQUES Chr: Samuel Palermo Track: Wireline	Session 18 SOCS FOR RECOGNITION & LEARNING Chr: Satoshi Shigematsu Track: SoC	Session 19 FREQUENCY SYNTHESIS AND TRANSMITTER TECHNIQUES Chr: Chun-Huat Heng Track: RF		
	16:00-16:20 (20min)	Break(Drinks & Refreshments)						
	16:20-18:00 (100min)		Session 20 ENERGY HARVESTING Chr: Takeshi Ueno Track: ACS	Session 21 OVERSAMPLING AND TIME-DOMAIN CONVERTERS Chr: Tsung-Heng Tsai Track: DC	Session 22 ENERGY-EFFICIENT TECHNIQUES FOR SOC Chr: Pei-Yun Tsai Track: SoC	Session 23 RF BUILDING BLOCKS Chr: Minoru Fujishima Track: RF		

Session 17: WIRELINE TRANSMITTER TECHNIQUES

Chair : Samuel Palermo, Texas A&M University
Co-Chair : Yasufumi Sakai, Fujitsu Laboratories Ltd.

14:20-14:45
S17-1 (4153)
A 32.75-Gb/s Voltage Mode Transmitter with 3-Tap FFE in 16nm CMOS
K. Chan{1}, K. Tan{1}, Y. Frans{2}, J. Im{2}, P. Upadhyaya{2}, S. Lim{1}, A. Roldan{1}, N. Narang{1}, C. Koay{1}, H. Zhao{1}, K. Chang{2}
{1}Xilinx Singapore, Singapore; {2}Xilinx, Inc., United States

14:45-15:10
S17-2 (4126)
A Model Predictive Control Equalization Transmitter for Asymmetric Interfaces in 28nm FDSOI
T. Kim, P. Bhargava, V. Stojanović
University of California, Berkeley, United States

15:10-15:35
S17-3 (4015)
A 6-to-32 Gb/s Voltage-Mode Transmitter with Scalable Supply, Voltage Swing, and Pre-Emphasis in 65-nm CMOS
W. Bae, H. Ju, K. Park, D. Jeong
Seoul National University, Korea

15:35-15:47
S17-4 (4177)
All-Synthesizable 6Gbps Voltage-Mode Transmitter for Serial Link
Y. Choi, K. Seong, B. Kim, J. Sim, H. Park
Pohang University of Science and Technology, Korea

15:47-15:59
S17-5 (4059)
A 5-8 Gb/s Low-Power Transmitter with 2-Tap Pre-Emphasis Based on Toggling Serialization
S. Kim, T. Kim, D. Kwon, W. Choi
Yonsei University, Korea

A 5-8 Gb/s Low-Power Transmitter with 2-Tap Pre-Emphasis Based on Toggling Serialization

Sung-Geun Kim, Tongsung Kim, Dae-Hyun Kwon, and Woo-Young Choi
Department of Electrical and Electronic Engineering, Yonsei University
Seodaemun-gu, Seoul 120-749, Korea
sgkim85@yonsei.ac.kr

***Abstract*—We demonstrate a low-power wireline transmitter with 2-tap pre-emphasis in which serialization is achieved by toggling serializer with data transition information extracted from parallel input data. This novel technique of serialization provides significantly reduced power consumption since it does not need the short pulse generation block required in the conventional serializer. In addition, the same data transition information can be directly used for implementing 2-tap pre-emphasize and, consequently, the need for the additional serializer required in the conventional pre-emphasis circuits can be eliminated, resulting in further reduced power consumption. A prototype transmitter realized in 65nm CMOS technology achieves energy efficiencies of 0.202 pJ/bit at 5 Gb/s and 0.3 pJ/bit at 8 Gb/s for 150 $mV_{pp,d}$ output voltage swing without pre-emphasis, and 0.252 pJ/bit at 5 Gb/s and 0.333 pJ/bit at 8 Gb/s with 2-tap pre-emphasis providing 6-dB equalization gain. To the best of our knowledge, these are the lowest energy efficiencies achieved for wireline transmitters realized in 65nm CMOS technology.**

Keywords—transmitter, low power transmitter, energy efficient, pre-emphasis, data transition information, toggling serializer

I. INTRODUCTION

The wireline bandwidth requirements for many high-performance Si systems ranging from portable devices to data center servers are continuously increasing. Furthermore, these requirements have to be satisfied without much increase in energy efficiency, making realization of high-speed and low-power wireline transmitters, which are responsible for a significant portion of the total transceiver power consumption, a great design challenge. In recently reported low-power wireline transmitters [1]-[3], large-ratio serialization has been used so that power consumption due to distribution of high-frequency clock signals can be reduced. Fig. 1 shows the block diagram of such a transmitter having the last stage serialization ratio of 4:1. Four parallel input data aligned with quadrature clock signals for avoiding the glitch problem are serialized with pulse signals. The width of each pulse signal should be same as the period of serializer output data, but generation and distribution of such short pulse signals having sufficiently fast rising and falling time consume a fair amount of power.

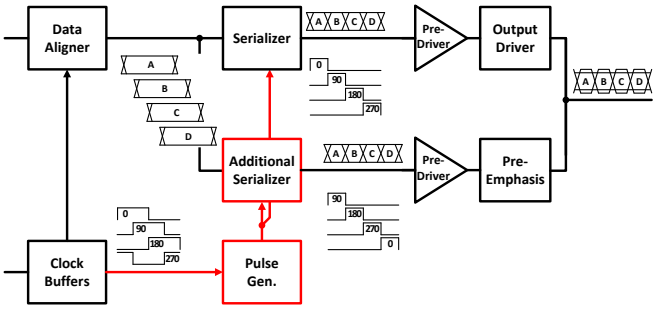

Fig. 1. Block diagram and timing diagram for a conventional transmitter having 4:1 serializer and 2-tap pre-emphasis.

Moreover, an additional serializer block, which receives 90 degree delayed pulse signals, is needed to make 1-bit delayed data for 2-tap pre-emphasis, resulting in considerable increase of the entire transmitter power consumption.

We propose a new transmitter structure in which serialization is realized by simply toggling serializer with data transition information extracted from parallel input data and, consequently, power consumption due to high-frequency pulse signal generation and distribution can be eliminated. Furthermore, the same data transition information can be directly used for implementing 2-tap pre-emphasis without any need for the duplicated serializer, resulting in additional power saving. With a prototype 5-8 Gb/s transmitter realized in 65nm CMOS technology, we demonstrate energy efficiencies of 0.202 pJ/bit at 5 Gb/s and 0.3 pJ/bit at 8 Gb/s for 150 $mV_{pp,d}$ output swing without pre-emphasis, and 0.252 pJ/bit at 5 Gb/s and 0.333 pJ/bit at 8 Gb/s for 300 $mV_{pp,d}$ output swing with 2-tap pre-emphasis that provides 6-dB equalization gain. To the best of our knowledge, these are the lowest energy efficiencies achieved for wireline transmitters realized in 65nm CMOS.

II. TRANSMITTER WITH TOGGLING SERILIZATION

Fig. 2 shows the block diagram and timing diagram of our transmitter which has a newly proposed 4:1 toggling serializer and the output driver with 2-tap pre-emphasis. In the toggling serializer, serialization is achieved in three steps. First, four input parallel NRZ data (A, B, C, D) are converted into RZ

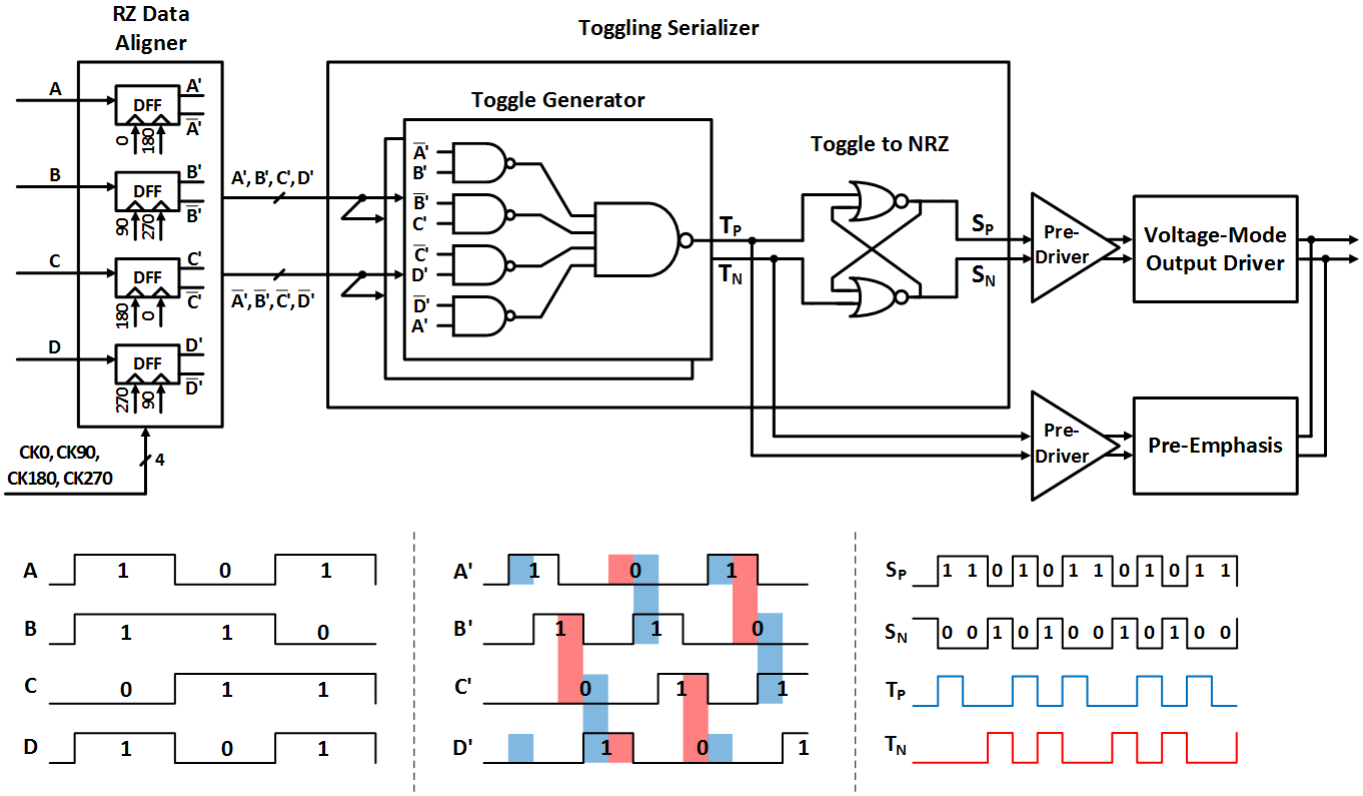

Fig. 2. Block diagram and timing diagram of our transmitter having toggling serializer and 2-tap pre-emphasis.

format (A', B', C', D') having 90 degree phase shift between adjacent input data with resettable DFFs and quadrature clock signals, as can be seen from timing diagrams in Fig. 2. Second, the toggle generator compares these RZ parallel input data and generates positive toggle signal, T_P, and negative toggle signal, T_N, where T_P indicates that positive serializer output (S_P) should be toggled from 0 to 1 and T_N indicates S_P should be toggled from 1 to 0. For negative serializer output (S_N), T_P indicates that S_N should be toggled from 1 to 0 and T_N indicates S_N should be toggled from 0 to 1. The required logic operations for T_P and T_N are

$$T_P = \overline{\left(\left(\overline{A'} \cdot B'\right) \cdot \left(\overline{B'} \cdot C'\right) \cdot \left(\overline{C'} \cdot D'\right) \cdot \left(\overline{D'} \cdot A'\right)\right)}, \quad (1)$$

$$T_N = \overline{\left(\left(A' \cdot \overline{B'}\right) \cdot \left(B' \cdot \overline{C'}\right) \cdot \left(C' \cdot \overline{D'}\right) \cdot \left(D' \cdot \overline{A'}\right)\right)}. \quad (2)$$

Finally, S_P and S_N can be determined from T_P and T_N by simple SR-latch operation.

The RZ data aligner block is implemented by replacing DFFs in the conventional data aligner with resettable DFFs. The amount of power needed for implementing RZ data is much smaller than the power needed for the pulse generator in the conventional serializer since the pulse width of RZ data is twice wider than the quadrature pulse signals. In addition, T_P and T_N can be directly supplied to the pre-emphasis block as they contain the information when the transmitter output needs to be pre-emphasized.

For contrast, for conventional low-power transmitters, implementing pre-emphasis with voltage-mode output driver (VMDRV) is difficult and various circuit techniques have been proposed for pre-emphasis such as hybrid current-mode [4], resistive divider [5], channel-shunting [6], and impedance-modulation [7]. In these, pre-emphasis tap coefficients are controlled with output stage segmentation [5-7], which needs additional serializer or complex high-speed pre-drivers and, consequently, increases power consumption.

In our transmitter, simple current boosting 2-tap pre-emphasis with VMDRV [8] is used with toggle signals T_P, T_N as shown in Fig. 3. For the positive transmitter output, TX_P, the pre-emphasis circuit pushes the boosting current, I_{EQ}, to the output node with T_P, and pulls I_{EQ} from the output node with T_N. For the negative output, TX_N, it pushes I_{EQ} with T_N and pulls I_{EQ} with T_P, where I_{EQ} is controlled with a replica controller. The VMDRV output swing can be controlled from 100 to 300 $mV_{pp,d}$ by a regulator and the output impedance is matched to 50 Ohm with a replica impedance controller.

Because TX_P and TX_N are pre-emphasized with current boosting rather than de-emphasis, the output signals maintain the DC voltage level even with different equalization gain. The pre-emphasis boosting current for target equalization gain is set by an external control with a replica pre-emphasis current controller, and bias voltages VEQP and VEQN are fed into the pre-emphasis block. By using toggle signals from the serializer and achieving current boosting with the impedance control,

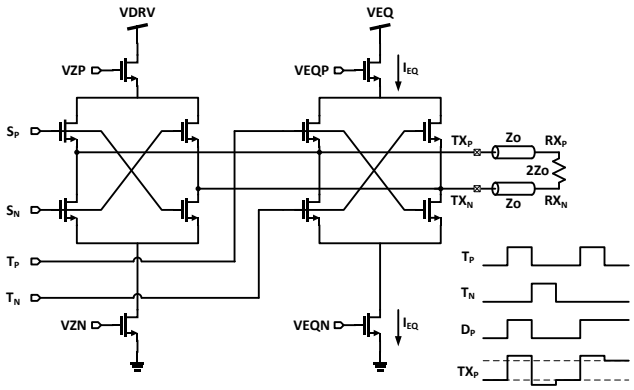

Fig. 3. Voltage-mode output driver (VMDRV) with pre-emphasis using toggle signals.

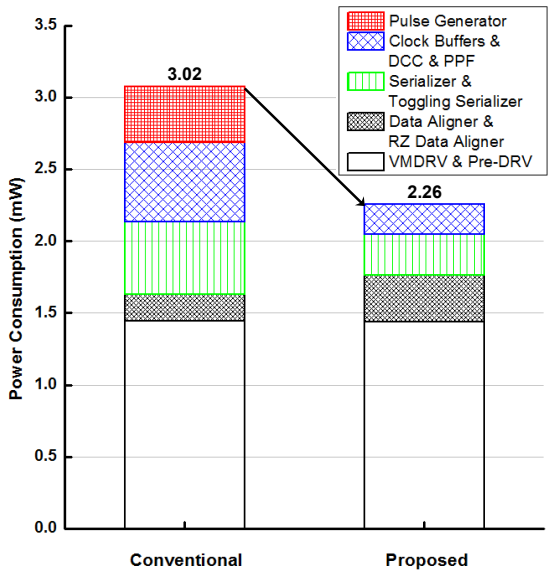

Fig. 4. Comparison of simulated power consumption at 8 Gb/s.

only simple buffers are needed for the pre-driver. All the transistors in the impedance controller and the pre-emphasis current controller are 16 times smaller than those in VMDRV and pre-emphasis, respectively, for power saving.

In Fig. 4, simulated power consumptions are compared for 8-Gb/s transmitters with 4:1 serializer realized in 65nm CMOS technology based on our newly proposed and the conventional structures. Both transmitters receive external differential clocks and generate quadrature clocks with polyphaser filter (PPF) and duty cycle corrector (DCC). 4:1 serializer and the pulse generator in the conventional transmitter are composed of CMOS logic gates having the same fan-out strength of 2 for fair comparison. Our transmitter does not need any pulse generator, nor any extra serializer for pre-emphasis. In addition, the number of required clock buffers is smaller. As can be seen in the figure, our transmitter consumes 25% less power.

III. Experimental Results

A prototype transmitter is realized in Samsung 65-nm CMOS technology. Fig. 5 shows the microphotograph of the

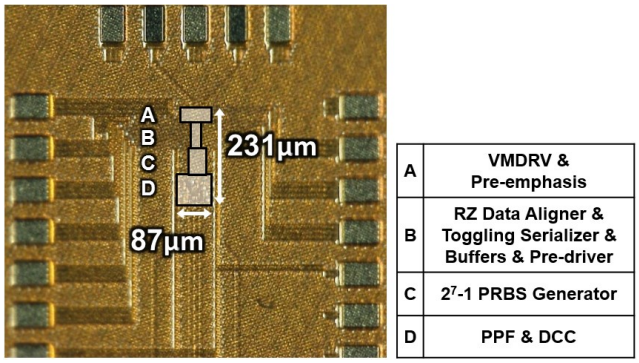

Fig. 5. Chip microphotograph.

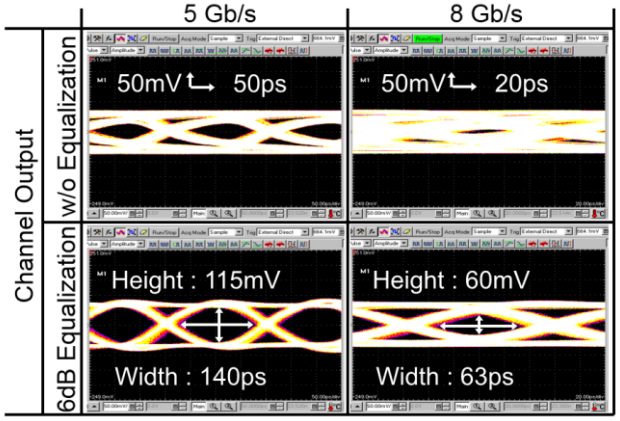

Fig. 6. Measured eye diagrams of channel output without pre-emphasis and with 6-dB gain pre-emphasis at 5 and 8 Gb/s.

fabricated chip. The active chip area is 87x231 µm^2 including an on-chip 2^7-1 PRBS generator. The fabricated chip is mounted on FR4 PCB and wire-bonded for measurement.

The transmitter is tested with 5 to 8 Gb/s 2^7-1 PRBS data. The supply voltage is reduced as much as possible for each data rate as long as the transmitter output eye provides 110mV$_{pp,d}$ height and 0.6 UI width, except for VMDRV and pre-emphasis whose supply voltages are fixed at 0.5 V. Fig. 6 shows measured eye diagrams at 5 Gb/s and 8 Gb/s with and without pre-emphasis after transmission through 40 cm FR4 trace and 50 cm SMA cable, which have measured loss of 7.4 and 10.7 dB at 2.5 and 4 GHz, respectively. For these measurements, transmitter output voltages are set to 150 mV$_{pp,d}$ without pre-emphasis and 300 mV$_{pp,d}$ with 6-dB equalization gain.

Fig. 7 shows measured energy efficiencies of our transmitter at different data rates in comparison with previously reported transmitters realized in 65nm CMOS [1-3]. Our transmitter achieves energy efficiency of 0.202 to 0.3 pJ/bit for 5 to 8 Gb/s without pre-emphasis and 0.252 to 0.333 pJ/bit for 5 to 8 Gb/s with pre-emphasis, respectively. Clearly, our transmitter has the lowest energy efficiency.

Table I gives more detailed performance comparison for various transmitters realized in 65nm CMOS [1-3]. For direct comparison, the power consumption of the total transmitter is divided by the output swing voltage. This comparison confirms

TABLE I. PERFORMANCE SUMMARY AND COMPARISON

	[1]	[2]	[3]	This work		
Technology	65 nm	65 nm	65 nm	65 nm		
Supply Voltage (V)	0.6-0.8	0.45-0.7	0.75-1	0.8 [5Gb/s], 0.85 [6Gb/s], 1 [8Gb/s]		
Dara Rate (Gb/s)	4.8-8	1-6	8-16	5-8		
Output Swing ($mV_{pp,d}$)	100-200	200	100-300	100-300		
Energy Efficiency w/o PE (pJ/bit) [Data rate, Swing Voltage]	0.3 [6.4Gb/s, 150$mV_{pp,d}$]	0.31 [6Gb/s , 200$mV_{pp,d}$]	0.65 [8Gb/s, 300$mV_{pp,d}$]	0.202 [5Gb/s, 150$mV_{pp,d}$]	0.22 [6Gb/s, 150$mV_{pp,d}$]	0.3 [8Gb/s, 150$mV_{pp,d}$]
Energy Efficiency w/o PE per Output Voltage Swing (pJ/bit/V)	2	1.55	2.17	1.35	1.47	2
Energy Efficiency w/ PE (pJ/bit) [Data rate, Swing Voltage]	N/A	N/A	0.81 [12Gb/s, 300$mV_{pp,d}$]	0.252 [5Gb/s, 300$mV_{pp,d}$]	0.269 [6Gb/s, 300$mV_{pp,d}$]	0.333 [8Gb/s, 300$mV_{pp,d}$]
Channel Loss	N/A	N/A	-12dB @ 6GHz	-7.4dB @ 2.5GHz	-8.5dB @ 3GHz	-10.7dB @ 4GHz

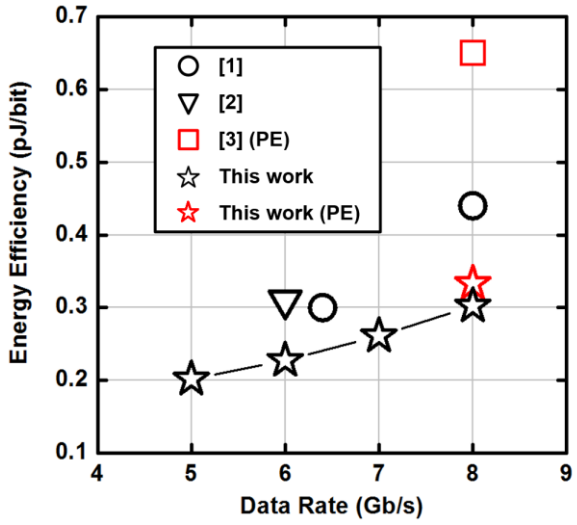

Fig. 7. Measured energy efficiencies at various data rates for our transmitter and other transmitters.

that our transmitter with 4:1 toggling serializer efficiently reduces power consumption.

IV. CONCLUSION

We proposed a low-power wireline transmitter having a novel toggling serializer. For low-power consumption, parallel data are serialized with toggle signals extracted from parallel input data. Furthermore, the direct use of toggle signals for pre-emphasis as well as current boosting equalization with impedance control significantly reduces circuit complexity and power consumption. With these, our transmitter achieves the lowest energy efficiency among wireline transmitters realized in 65nm CMOS technology.

ACKNOWLEDGMENT

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