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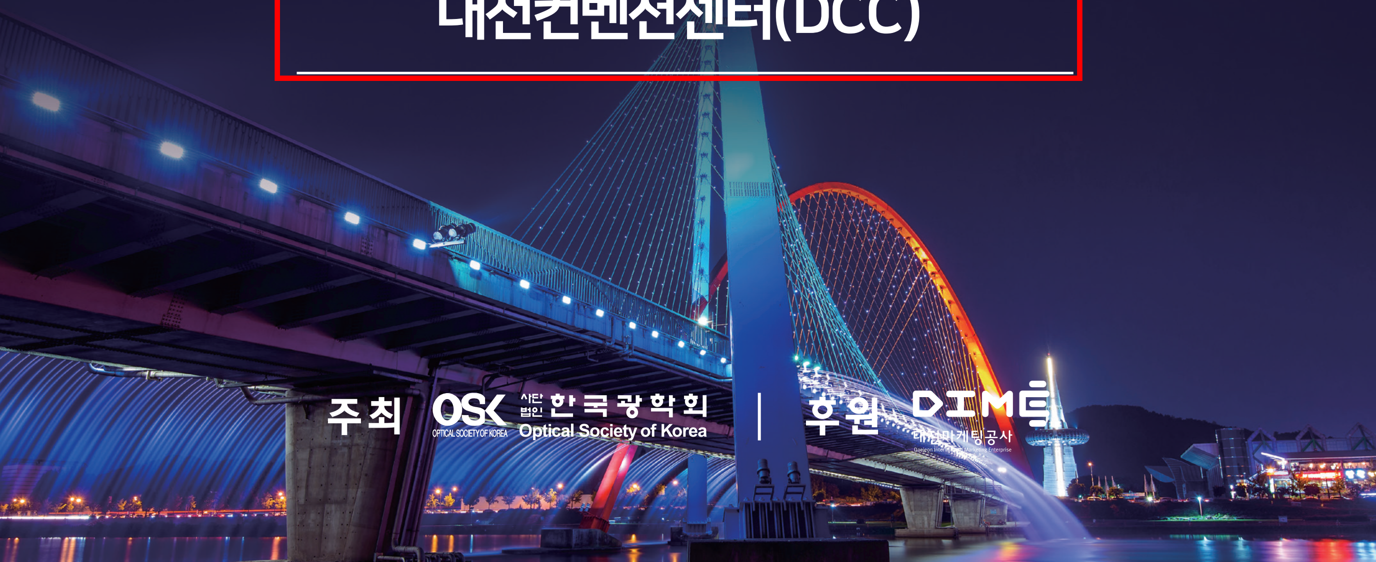
제33회 한국광학회 정기총회 및 2022 동계 학술발표회

OptoWin 2022 광산업전시회

2022. 2. 16(수) ~ 18(금)

대전컨벤션센터(DCC)



주최 OSK OPTICAL SOCIETY OF KOREA 사단법인 한국광학회 Optical Society of Korea | 후원 DIME 대전마케팅공사 Daejeon International Marketing Enterprise

일 정 표

2022년도 동계학술발표회 일정표

Ⅰ=광과학 Ⅱ=광기술 Ⅲ=디지털홀로그래피 및 정보광학 Ⅳ=양자전자 Ⅴ=포토닉스 Ⅵ=바이오포토닉스 Ⅶ=디스플레이 Ⅷ=양자광학 및 양자정보 Ⅸ=리소그래피

2022년 2월 16일(수, W)

시간 \ 장소	101호 (A)	102호 (B)	103호 (C)	104호 (D)	105호 (E)	106호 (F)	107호 (G)	컨퍼런스홀 (H, 3층)
09:00~	Registration							
10:30~12:00			디지털홀로그래피 및 정보광학 I 좌장: 이승열(경북대) W1C-III	양자전자 I 좌장: 김종환(POSTECH) W1D-IV		포토닉스 I 좌장: 김훈(KAIST) W1F-V		양자컴퓨터와 양자시뮬레이터 I 좌장: 문한섭(부산대) W1H-VIII-S
12:00~13:30	Lunch							
13:30~15:00	광과학 I 좌장: 송영민(GIST) W1A-I	광기술 I 좌장: 박성찬(단국대) W1B-II	디지털홀로그래피 및 정보광학 II 좌장: 정진수(KETI) W2C-III	양자전자 II 좌장: 장민석(KAIST) W2D-IV		포토닉스 II 좌장: 박연상(충남대) W2F-V	윤태훈 고문 은퇴 기념세션 좌장: 이길주(부산대) W1G-VII-S	양자컴퓨터와 양자시뮬레이터 II 좌장: 박희수(KRISS) W2H-VIII-S
15:00~15:15	Break time							
15:15~16:45	광과학 II 좌장: 이승우(고려대) W2A-I	광기술 II 좌장: 정미숙(산기대) W2B-II	디지털홀로그래피 및 정보광학 III 좌장: 임용준(ETRI) W3C-III	양자전자 III 좌장: 이관일(KIST) W3D-IV		바이오포토닉스 I 좌장: 김기현(POSTECH) W3F-VI	디스플레이 I 좌장: 조남성(ETRI) W2G-VII	양자컴퓨터와 양자시뮬레이터 III 좌장: 한상욱(KIST) W3H-VIII-S
16:45~17:00	Break time							

시간 \ 장소	1층 전시홀 (111호)
17:00~18:00	Poster Session I 광과학 (WP-I 1~8), 광기술 (WP-II 1~8), 디지털홀로그래피 및 정보광학 (WP-III 1~2), 양자전자 (WP-IV 1~6), 포토닉스 (WP-V 1~7), 바이오포토닉스 (WP-VI 1~15), 디스플레이 (WP-VII 1~7), 양자광학 및 양자정보 (WP-VIII 1~4), 리소그래피(WP-IX 1~2)

시간 \ 장소	3층 컨퍼런스홀
17:00~18:00	이사회
18:00~18:10	Break time
18:10~19:00	평의원회

W2F-V : 포토닉스 II

좌장: 박연상(충남대학교)

106호 (F), 02월 16일 (수) 13:30 - 14:45

13:30 (초청강연) **W2F-V.01**

Development of DSP-IC Operation Board for Processing 100-Gbps PAM4 Signals and Its Applications

Yun Seokjun, Han Youngtak, Shin Janguk (ETRI), Kim Seoktae (Luvantix ADM), Park Sangho, Lee Seoyoung, BAEK YONGSOON (ETRI)*

14:00 **W2F-V.02**

IM/DD 광전송에서 단일 PD기반 QAM-PIRFSK신호 전송 기법

HA Inho, LEE Jeoungmoon, PARK Jinwoo, HAN Sang-Kook (Yonsei University)*

14:15 **W2F-V.03**

Clipping Tone 변조 레이저 다이오드를 이용한 채널에 강인한 무선 광 전송 기법 연구

CHOI Jae-Young, HAN Sang-Kook, HYUN Young-jin (Yonsei University)*

14:30 **W2F-V.04**

An Equivalent Circuit Model for 850nm VCSELs Based on Measured S-parameters

KIM Kihun (Yonsei University), KIM Jaeyoung (Qualitas Semiconductor Co.), KIM Junseo, CHOI Woo-Young (Yonsei University)*

An Equivalent Circuit Model for 850nm VCSELs Based on Measured S-parameters

Kihun Kim[1*], Junseo Kim[1], Jaeyoung Kim[2], and Woo-Young Choi[1]
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***Abstract*—This paper presents an equivalent circuit model for Vertical-Cavity Surface-Emitting Lasers (VCSELs) implemented in Verilog-A, a standard circuit simulation tool. Our model accounts for electrical as well as optical characteristics of a VCSEL, and allows an easy and accurate simulation of VCSEL output when it is modulated by an electrical circuit.**

I. Introduction

Vertical-Cavity Surface-Emitting Lasers (VCSELs) are very attractive for short-distance optical interconnect solutions especially in data center applications. They are capable of very high-bandwidth optical data transmission over multi-mode fiber with high cost-effectiveness. However, VCSELs have intrinsic nonlinear modulation characteristics, which make designing of efficient driver circuits quite challenging especially for PAM4 applications. Although the VCSEL rate equations can be used for modeling VCSEL modulation characteristics[1, 2], they are complicated and not compatible with the standard electronic circuit design environment. In this paper, we demonstrate a VCSEL equivalent circuit, which is accurate and easy to use.

II. VCSEL Modelling

Fig. 1 shows the proposed equivalent circuit for the VCSEL. The left side accounts for the VCSEL electrical characteristics and the RLC circuit in the right side represents the two-pole transfer function for the VCSEL modulation frequency response.

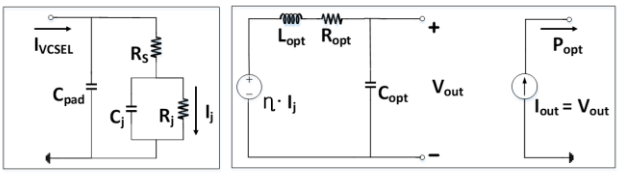


Fig. 1 VCSEL equivalent circuit model

The numerical values for the circuit elements within the equivalent circuit can be determined by matching measured S11 and electro-optical S21 parameters with the simulated results of the equivalent circuit in Verilog-A as shown in Fig. 2. For the measurement, a commercial VCSEL is measured with a light component analyzer at several different bias currents. For good matching, bias-dependent circuit parameter values are used with the fourth-order polynomial fitting functions.

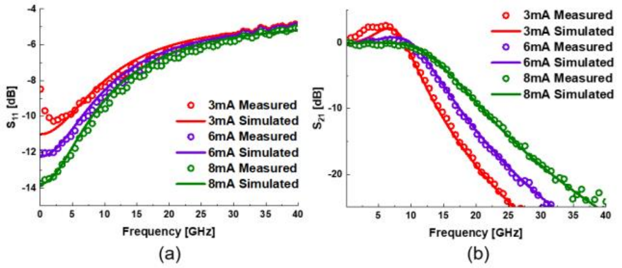
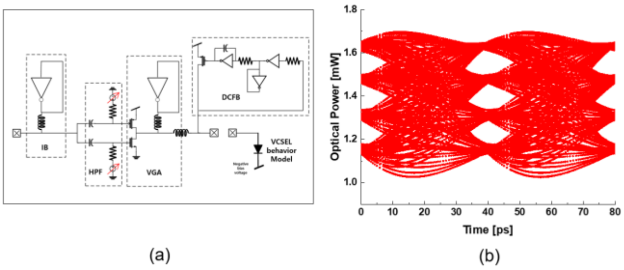


Fig. 2 Measured and simulated (a) S_{11} and (b) electro-optical S_{21}

Fig. 3(a) shows the block diagram of the VCSEL transmitter including the CMOS driving circuit. The VCSEL driver implemented in 28nm CMOS technology is designed to produce pre-distorted VCSEL driving currents so that the resulting 50Gbps PAM4-modulated VCSEL optical output signals has enhanced Level Separation Mismatch Ratio (RLM) performance as shown in Fig. 3(b). The entire simulation is done in Cadence Spectre, a standard IC design environment. More details of our VCSEL modeling will be presented.



[Fig. 3] (a) Block diagram and (b) PAM4 simulation result of VCSEL behavior model with VCSEL driver

Reference

[1] B. Wang *et al.*, "Comprehensive vertical-cavity surface-emitting laser model for optical interconnect transceiver circuit design", Optical Engineering, 55(12), p.126103, 2016.
[2] C. Zhang *et al.*, "A Compact VCSEL Model for High-Speed Optical Interconnect Design." *Laser Applications Conference*. Optical Society of America, 2021.