www.theieie.org

22nd RF/아날로그 회로 WORKSHOP

RF/Analog Circuit Workshop

- **일 정** : 2022년 9월 22일(목) ~ 24일(토)
- **장 소** : 라마다프라자 제주호텔 (제주시)
- **주 관** : 강원대학교, 한국전자통신연구원
  차세대반도체 불량분석 및 품질관리 전문인력양성사업단
  차세대 시스템반도체 설계 전문인력양성사업단
- **주 최** : 대한전자공학회 RF집적회로연구회
- **공동주최** : 한국전자파학회 (마이크로파 연구회)
  Seoul Chapter of IEEE SSCS, EDS, CAS, MTT-S
- **후 원** : 삼성전자, LX세미콘, 포인트투테크놀로지, SK하이닉스, 라온텍, 빌리브마이크론, 시놉시스코리아, 실리콘마이터스, 실리콘알앤디, 오픈엣지테크놀로지, 텔리닥스 반도체, 하이딥, 한국전자기술연구원, 현대 모비스, 케이던스코리아, 키사이트테크놀로지스, 안리쓰코퍼레이션, 에스비솔루션, 파이칩스
- **웹사이트** : http://rf22nd.ieieweb.org

IEIE 대한전자공학회 KNU 강원대학교 ETRI

2022년 9월 22일(목요일)

14:00~15:30 ■ Session 1: RF & mm-Wave Circuit Techniques 1. High Power, Energy-Efficient, and Broadband SiGe HBT Power Amplification for Emerging 6G Wireless Transmitter Front-End-Module 2. mm-Wave CMOS Beamforming RFIC 3. Broadband Wireless Radio and Its Relevance to Biomedical Applications	**좌장 : 권익진 교수(아주대)** **주인찬** 교수(아주대) **김철영** 교수(충남대) **김주성** 교수(한밭대)
14:00~15:30 ■ Session 2: Circuits & Systems for Wireline & Wireless Communication 1. High-Speed Interconnect Technology 2. New SerDes Technologies for Optical Communication 3. High-Speed PAM4 CDR RX Design Considerations	**좌장 : 김지훈 교수(이화여대)** **진태환** 박사(퀄리타스반도체) **박진호** 대표(포인투테크놀로지) **이순섭** 박사(오픈엣지)
15:30~15:45 ■ COFFEE BREAK	
15:45~16:30 ■ POSTER SESSION	
16:40~17:30 ■ Plenary Session · Two Questions for the Data-Driven World	**좌장 : 황인철 교수(강원대)** **조병학** 교수(KAIST)
18:00~20:00 ■ 개회식 · 개회사 · 환영사 · 축 사 · RF집적회로 기술인의 밤	**사회 : 제민규 교수(KAIST)** **황인철** 운영위원장 RF 집적회로연구회 **김영진** 위원장 대한전자공학회 **서승우** 회장

2022년 9월 23일(금요일)

10:45~12:15 ■ Session 3: Analog & Mixed-Signal Circuit Techniques 1. 디스플레이 최근 현황과 시스템 반도체의 기술 대응 2. 초저면적 고해상도 Display Driver IC 최신 설계 기법 3. Design Automation for SAR ADCs	**좌장 : 이정협 교수(DGIST)** **전현규** 이사(LX세미콘) **김현식** 교수(KAIST) **서민재** 교수(가천대)
10:45~12:15 ■ Session 4: Circuits & Systems for Display, Sensing, and Medical Applications 1. A Low-Power High-Resolution CMOS Sensor System for IoT Applications 2. Techniques for Efficient Temperature Sensor Design 3. High Efficiency Ultrasound Transducer Driver Circuits	**좌장 : 배준성 교수(강원대)** **박수진** 박사(ETRI) **정완영** 교수(KAIST) **지동우** 교수(아주대)
12:15~13:15 ■ LUNCH	
13:15~14:05 ■ Plenary Session · Circuit Solutions for Sub-THz Transceivers to Overcome the Technology Limitations	**좌장 : 제민규 교수(KAIST)** **이상국** 교수(KAIST)
14:05~14:20 ■ COFFEE BREAK	
14:20~15:50 ■ Session 5: Circuits & Systems for 6G & B5G 1. A Digital-IF RF Receiver 2. Blocker-Tolerable RF Front-End Design for Next Generation Cellular Application 3. 대용량 무선 백홀용 sub-THz 대역 물리계층 기술	**좌장 : 고승훈 교수(광운대)** **성바로샘** 수석(삼성전자) **한정환** 교수(충남대) **현석봉** 박사(ETRI)
14:20~15:50 ■ Session 6: Circuits & Systems for Emerging Applications 1. Micro-display Circuit & Systems for XR (AR/VR/MR) Devices 2. MRAM In-Memory Computing 3. An All-in-One Fingerprint Security IC for Biometric Payment Cards	**좌장 : 이규호 교수(UNIST)** **김보은** 대표(라온텍) **정승철** 전문(삼성종합기술원) **장지수** 수석(삼성전자)
16:00~17:00 ■ 폐회식 · 폐회사 · 우수포스터논문 시상 · 행운권 추첨	**사회 : 강명곤 교수(한국교통대)** RF집적회로연구회 **김영진** 위원장 **권구덕** 학술위원장

2022년 9월 24일(토요일)

10:00~12:00 ■ RF/아날로그 회로 포럼 · 참석대상 : 연구회 전문위원 전체	**RF 집적회로연구회**

System
u Je
er for
g SAR
Kim,
Base
wan Han
r for 5G
im, and
mic
etector
Tae Kim,
out
nveyor

47. An Ultra-Compact Charge Compensator of Self-Capacitive Touch Screen Panel for foldable AMOLED display
    저자 : Junmin Lee, Hyoyoung Kim, Gaeun Ju, Juwon Ham, and Seunghoon Ko
    소속 : Kwangwoon University

48. An eFlash-Based Computation-in-Memory for Edge Computing
    저자 : Injun Choi, Jongyoon Choi, Donghyeon Yi, ByeongSeon Choi, and Minkyu Je
    소속 : KAIST

49. FMCW Generator for High Range Resolution Radar
    저자 : Eun-Ho Song, Hyun-Yeop Lee, Ho-Seon Baek, Seong-Tae Kim, Choon-Sik Cho, Yun-seong Eo and Young-Jin Kim
    소속 : Korea Aerospace University

50. 4 bit 0.5 GSs flash ADC for UWB application
    저자 : Hyun-Yeop Lee, Ho-Seon Baek, Seong-Tae Kim, Eun-Ho Song and Young-Jin Kim
    소속 : Korea Aerospace University

51. Analog Spike Detection Methods for Spike Sorting
    저자 : Vincent Lukito and Minkyu Je
    소속 : KAIST

52. An observation of channel potential according to the thickness change of blocking oxide in 3D NAND flash memory ONF structure
    저자 : Sunghyun Woo, and Myounggon Kang
    소속 : Korea National University of Transportation

53. Analysis of Ring Oscillator Circuit Operation Characteristics by Total Ionizing Dose Effect
    저자 : Jongwon Lee, and Myounggon Kang
    소속 : Korea National University of Transportation

54. Channel potential analysis to find optimal Remanent Polarization (Pr) and Saturation Polarization (Ps) in 3D NAND Charge Trap Flash using Ferroelectric (CTF-F) structure
    저자 : Jihwan Lee, and Myounggon Kang
    소속 : Korea National University of Transportation

55. Physical based ReRAM Cell Compact Modeling using Circuit Schematic
    저자 : Hyunju Kim, Jongwon Lee, and Myounggon Kang
    소속 : Korea National University of Transportation

56. The Analysis of Lateral Migration at 3D NAND Charge Trap Flash Memory by tapering
    저자 : Jaewoo Lee, and Myounggon Kang
    소속 : Korea National University of Transportation

57. The Comparison of Single Event Upset in structure of Gate All Around (GAA)
    저자 : Yunjae Kim, and Myounggon Kang
    소속 : Korea National University of Transportation

58. Study on Direct Digital Frequency Synthesis
    저자 : Jae-Yun Park, †Su-Hyeon Kim, Seong-Gyul Kim, Jin-Won Hyun, Yeon-Su Kim and Jae-Won Nam
    소속 : Seoul National University of Science and Technology

59. A 6.5-10GHz CMOS Power Amplifier For UWB
    저자 : Seong-Tae Kim, Hyun-Yeop Lee, Ho-Seon Baek, Eun-Ho Song and Young-Jin Kim
    소속 : Korea Aerospace University

60. Inverter-based 50Gbps PAM4 CMOS VCSEL Driver for Optical Interconnection
    저자 : Jun-Seo Kim[1], Ki-Hun Kim[1], Tae-Hwan Jin[2], and Woo-Young Choi[1]
    소속 : Yonsei University[1], Qualitas Semiconductor[2]

Inverter-based 50Gbps PAM4 CMOS VCSEL Driver for Optical Interconnection

Jun-Seo Kim[1], Ki-Hun Kim[1], Tae-Hwan Jin[2], and Woo-Young Choi[1]
Department of Electronical and Electronic Engineering
Yonsei University[1], Seoul, Korea
Qualitas Semiconductor[2], Seongnam-si, Korea
Email: kjs49620@yonsei.ac.kr

***Abstract*— An inverter based laser diode driver for short-reach optical interconnect with 850nm Vertical-Cavity Surface-Emitting Laser(VCSEL) is presented. The VCSEL driver consists of T-coils with ESD protection, 50-ohm termination, Signal Buffer(SB), Programmable Gain Amplifier(PGA), and DC current source with the DC feedback topology. These are based on inverter-type g_m/g_m amplifiers which can be controlled via I^2C. The circuit is designed in 14nm FinFET to drive 12.5GHz VCSEL for 50Gbps PAM4 operation.**

Keywords—Driver, 850nm VCSEL, PAM4, 50Gbps

I. Introduction

High-speed interconnects in datacenters and High-Performance Computing (HPC) applications are currently of great technological and commercial interests. Optical interconnection using Vertical-Cavity Surface-Emitting Lasers (VCSELs) is a promising solution for these applications [1]-[3] as VCSEL is a low-cost and energy-efficient light source. 850nm VCSEL is suitable for short-reach interconnection in HPCs or datacenters. Pulse Amplitude Modulation 4-level (PAM4) is a highly preferable method to increase interconnect bandwidth [4]. In this paper, a 50Gbps PAM4 VCSEL driver for a commercial VCSEL having 12.5 GHz optical modulation bandwidth is designed in 14nm FinFET technology.

II. Design of Building Block

Fig. 1 shows the schematic of g_m/g_m amplifier and the VCSEL driver. Inverter-type g_m/g_m amplifiers have a relatively low Total Harmonic Distortion (THD) compared to other inverter-type topologies, and easily allows the voltage gain adjustment [5]. Because of these, the gm/gm amplifiers are used as a main topology for our VCSEL driver. Additionally, the amplifier bandwidth is extended by using a shunt-peaking inductor in each amplifier's load.

Input and output stages have T-coils to compensate for bandwidth degradation caused by ESD protection. Programmable $1/g_m$ loads are placed at input stage for 50-ohm termination and self-bias voltage with half VDD. Signal Buffer (SB) is used for pole splitting between the input stage and the main amplifier. In order to adjust the amount of the modulation current applied to the VCSEL, $1/g_m$ load of Programmable Gain Amplifier (PGA) can be controlled by the 3-bit I^2C code. Also, inverter-type PGA can be controlled by the 4-bit I^2C code. The DC feedback-type voltage rectifier can control the amount of DC current flowing through the VCSEL by adjusting the negative bias voltage applied to the VCSEL cathode. Fig. 2 shows full-chip layout of the VCSEL driver.

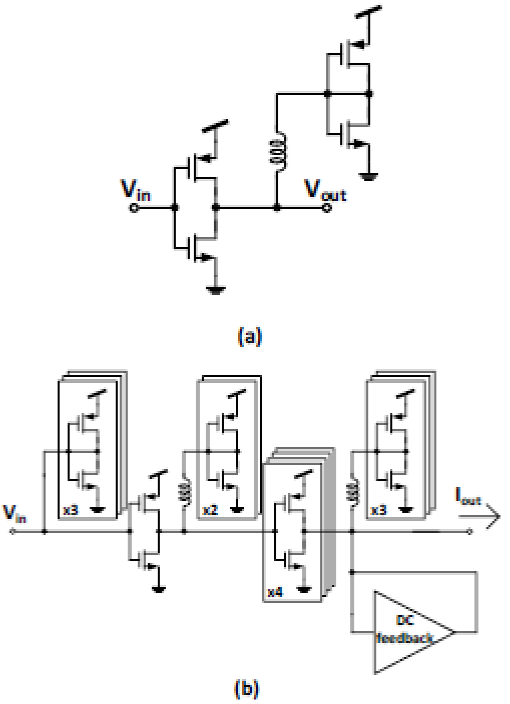

Fig. 1. Schematics of (a) g_m/g_m amplifier with shunt peaking inductance, (b) the VCSEL driver structure

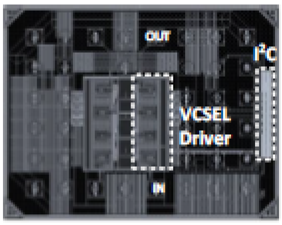

Fig. 2. Full-chip layout

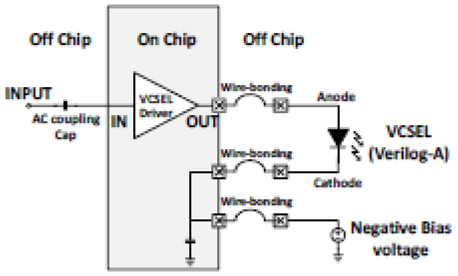

Fig. 3. Simulation test bench for realistic measurement setup

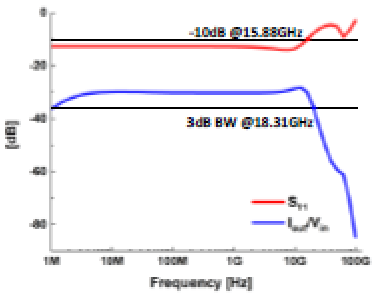

Fig. 4. Simulation results of S_{11} and AC simulation

III. SIMULATION RESUTLS

Fig. 3 shows the simulation test bench which is reflected realistic measurement set-up. At input side, AC coupling cap is used because VCSEL driver is implemented with inverter-type amplifiers which are needed half VDD bias voltage. At output side, the VCSEL driver is wire-bonded with VCSEL die. Therefore, wire-bond inductance model was used for test bench. The bond-wires create data dependent supply switching noise(SSN), ISI and it degrade the eye openings [6]. To reduce SSN, on-chip high frequency ground was implemented for VCSEL cathode. The VCSEL model is implemented in Verilog-A that can accurately emulate both electrical and optical characteristics of the target VCSEL.

Fig. 4 shows the simulated frequency responses for input impedance matching (S_{11}) and AC simulation of the VCSEL driver. For eye diagram simulation, 150mV$_{p-p}$ electrical signals with 50Gbps PAM4 2^{15}-1 PRBS are applied to the

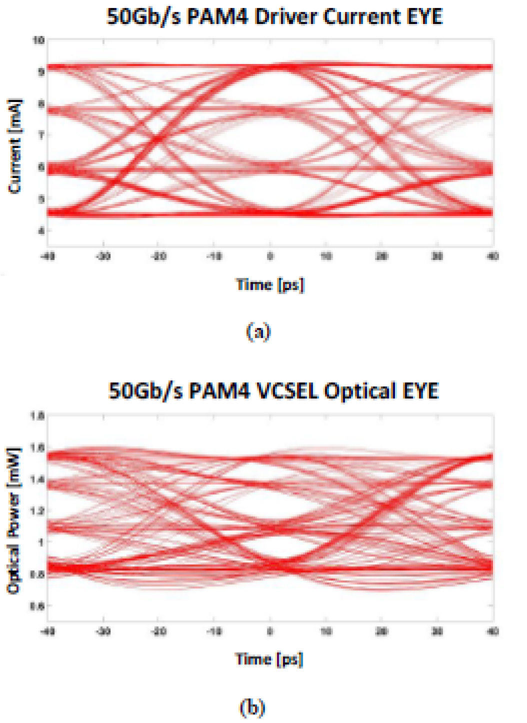

Fig. 5. Simulation results of (a) VCSEL Driver output current EYE, (b) Electrical to Optical conversion EYE

driver. Fig 5 (a), (b) shows the results. The simulation result shows 5mA$_{p-p}$ modulation current at 7mA DC current.

ACKNOWLEDGMENT

This research was supported by the Ministry of SMEs and Startups for small and medium-sized enterprises development program(S3031740).

REFERENCES

[1] I. Young, et al., "Optical I/O Technology for Tera-Scale Computing," IEEE J. Solid-State Circuit, vol. 45, no. 1, pp. 235-248, Jan. 2010.

[2] J. Jiang, et al., "100Gb/s Ethernet Chipsets in 65nm CMOS Technology" ISSCC Dig. Tech. Papers, pp. 120-122, Feb. 2013.

[3] He, Jian, et al. "Design of a PAM-4 VCSEL-Based Transceiver Front-End for Beyond-400G Short-Reach Optical Interconnects." IEEE Transactions on Circuits and Systems I: Regular Papers (2022).

[4] Cheng H, Yang Y, Liu T, Wu C (2022) Recent advances in 850 nm VCSELs for high-speed interconnects. Photonics 9(2):107

[5] K. Lakshmikumar, A. Kurylak, M. Nagaraju, R. Booth, and J. Pampanin, "A process and temperature insensitive CMOS linear TIA for 100 Gb/s/λ PAM-4 optical links," in Proc. IEEE Custom Integr. Circuits Conf., Apr. 2018, pp. 1–4.

[6] Ramani, Ajith Sivadhasan, Spoorthi Nayak, and Sudip Shekhar. "A differential push-pull voltage mode VCSEL driver in 65-nm CMOS." IEEE Transactions on Circuits and Systems I: Regular Papers 66.11 (2019): 4147-4157.