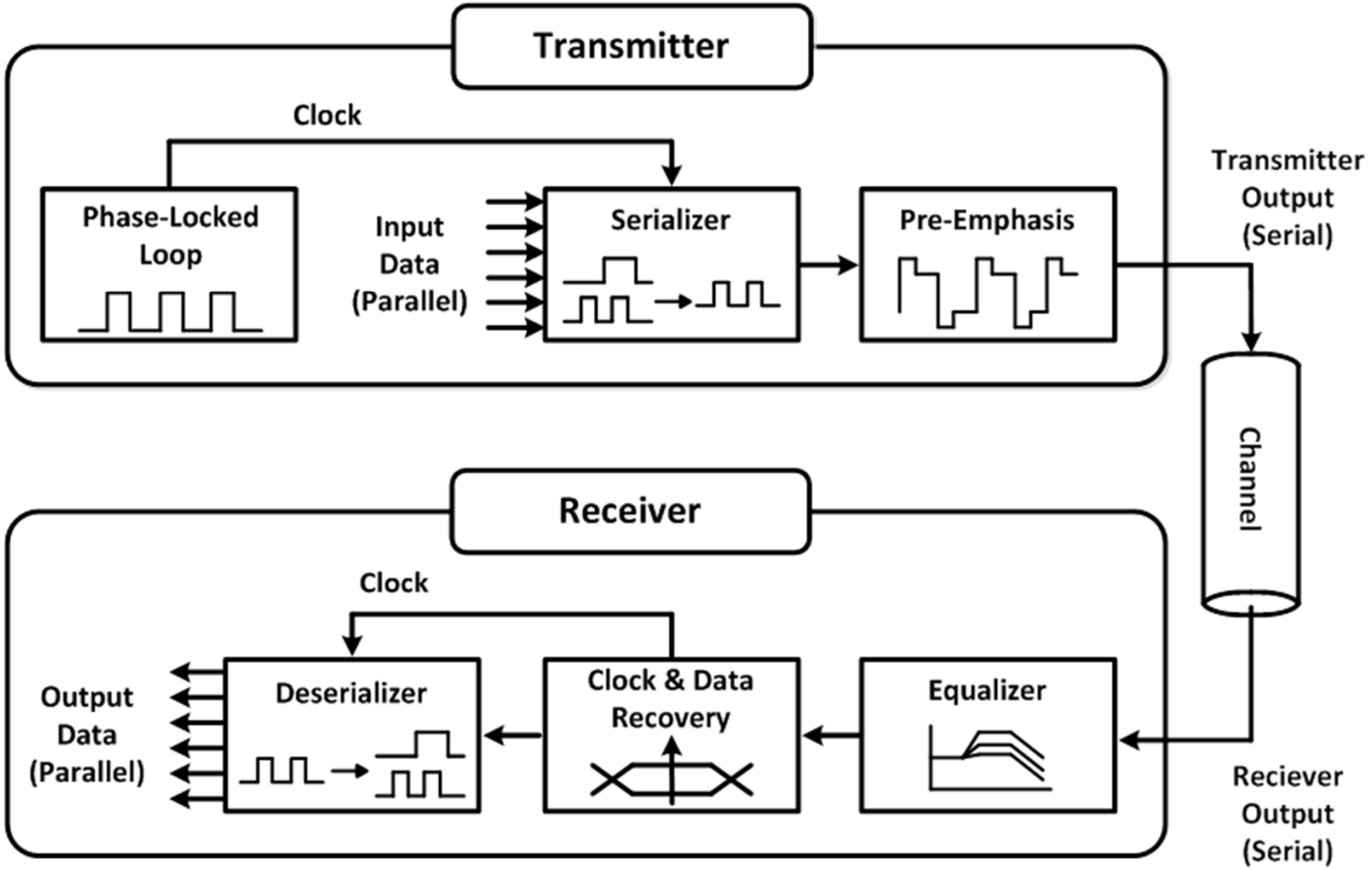
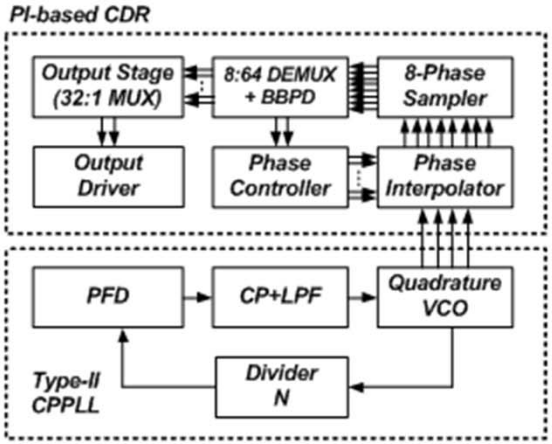
High Speed Circuits for Serial Link

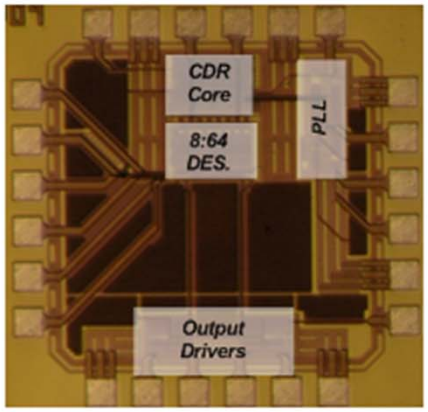


High Speed Circuits for Serial Link

Low-Power CDR Design



Overall Architecture

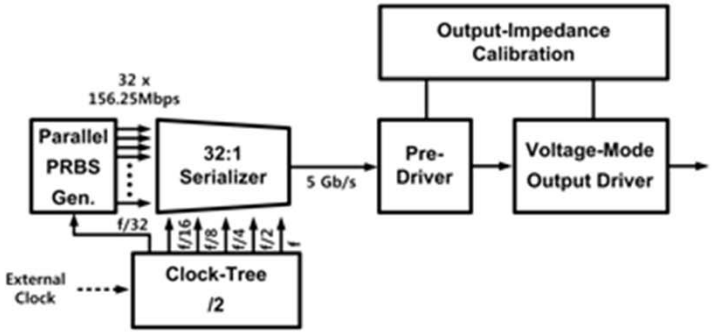


Chip Microphotograph

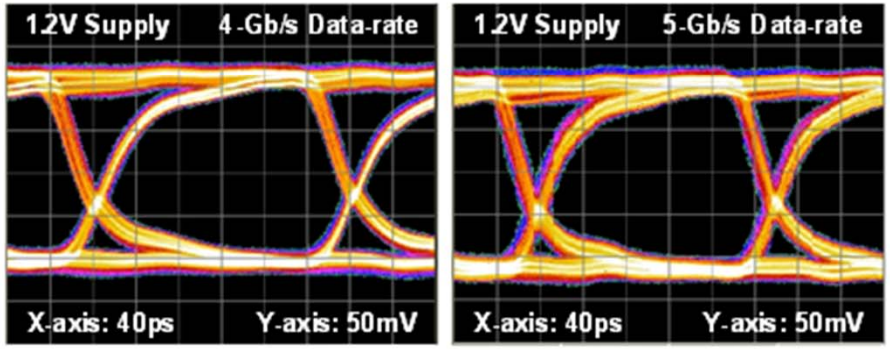
Low-Power CDR	
Technology	180nm CMOS
Data-rate (Pattern)	8 Gb/s (PRBS 31)
Power Consumption	38 mW
Power Efficiency	4.8 mW/Gb/s
Area	0.078 mm²

Chip Summary

Voltage-Mode Output Driver



Overall Architecture



Measured Eye-Diagram