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Novel 2-GHz-Range Fully Differential GaAs MESFET Phase-Locked Loops

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A novel 2-GHz-range fully differential phase-locked loop (PLL) is designed for clock generation applications. The PLL includes a differentially controlled voltage-controlled oscillator (VCO) with a tuning range of 1.74~3.40 GHz and a differential charge pump with improved hold characteristics. The PLL is implemented with Vitesse 0.5-μm GaAs MESFET (metal-semiconductor field-effect transistor) process. The experimental results show that the proposed PLL has a lock range of 1.74~3.40 GHz and a maximum VCO root-mean-square jitter of 9.0 ps (0.031 UI).

I. INTRODUCTION

In multi-link systems such as asynchronous transfer mode (ATM), it is more cost-effective to integrate several links into one high-speed serial link because it can reduce the system complexity. This requires high-speed phase-locked loops (PLLs) which provide the synthesized system clock for data serialization and de-serialization.

There have been many research efforts to increase the maximum PLL operating frequency and operating range and to reduce the voltage-controlled oscillator (VCO) output jitter [1–3]. Since the maximum operating frequency and operating range of a PLL are determined by the VCO and since the jitter characteristics are influenced by the VCO and the charge pump characteristics, most research efforts for high-speed PLL have focused on the VCO and the charge pump. Our goal is realizing a high-speed PLL with a wide lock-range and low jitter characteristics, and in order to achieve this goal, we come up with new circuit ideas for the VCO and the charge pump.

II. VOLTAGE-CONTROLLED OSCILLATOR

1. Conventional VCO

A ring oscillator-type VCO is widely used for implementing PLLs for system clock generation because it needs a very small chip area and it can produce high-frequency signals with large magnitudes suitable for digital system applications. There are many methods to control the oscillation frequency of the ring oscillator-type VCO, such as RC delay control [4], pull-down current control [5], and feedback loop coupling [6]. Among these, the feedback loop coupling method is the most suitable for high-speed PLL application because it has no oscillation frequency degradation due to the output loading capacitance.

Figure 1 shows a block diagram of a conventional VCO using the feedback loop coupling method. The VCO oscillation frequency (f_{OSC}) is tuned by the control signal (V_C) of the analog multiplexer (AMUX) which combines two loops having different loop delays. If it is assumed that the AMUX output V_z is linearly controlled by V_C and that V_C varies from 0 to 1, the AMUX output V_z can be expressed as

$$V_z = -[(1 - V_C)V_y + V_C V_x] \quad (1)$$

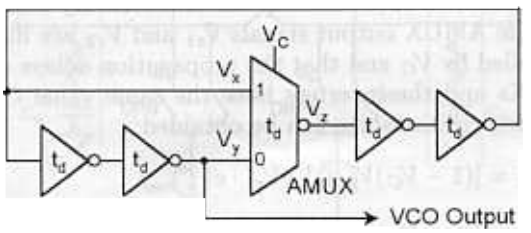

Fig. 1. Block diagram of a conventional VCO using the feedback loop coupling method.

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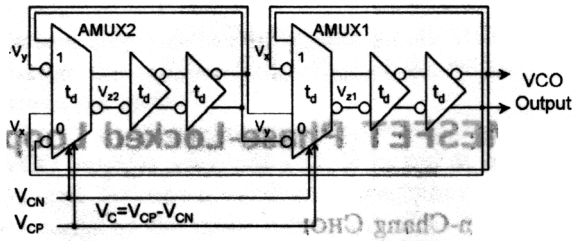

Fig. 2. Block diagram of the proposed VCO.

Also, the VCO tuning range can be expressed as

$$\frac{1}{2N_S t_d} \leq f_{OSC} \leq \frac{1}{2N_F t_d} \tag{2}$$

where N_S and N_F are the numbers of stages of the slow loop and the fast loop, respectively, and t_d is the propagation delay of the inverters and AMUX. With Eq. (2), the VCO tuning range shown in Fig. 1 can be determined as $1/(10t_d)\sim1/(6t_d)$. This type of VCO has several advantages. It is easy to determine the VCO tuning range and to design with a fully differential structure. Moreover, if the VCO output port is placed on the slow loop, as shown in the figure, the maximum f_{OSC} is not lowered by the output loading capacitance.

However, there is a limitation on increasing its tuning range because of the unstability of the AMUX. In Fig. 1, the delay difference between the two AMUX input signals is $2t_d$. When the VCO oscillates with its minimum f_{OSC}, its oscillation period (T_{OSC}) becomes $10t_d$, and the phase difference between the two AMUX inputs becomes $2\pi/5$. In the same way, when the VCO oscillates with its maximum f_{OSC}, T_{OSC} becomes $6t_d$, and the phase difference between the two AMUX inputs becomes $2\pi/3$. From this, the phase difference between two AMUX input signals is in the range of $2\pi/5\sim2\pi/3$. This can make the loop gain of the VCO very small and the oscillation ceased because as the AMUX input phase difference increases, the magnitude of the AMUX output decreases [7].

2. Proposed VCO

Figure 2 shows a block diagram of a new VCO structure [7,8]. It has two identical loops, each of which consists of one AMUX and several inverters. Two loops are combined with each other by the AMUXs. By assuming that the AMUX output signals V_{z1} and V_{z2} are linearly controlled by V_C and that the propagation delays of the AMUXs and the inverters have the same value t_d, the following relationships can be obtained:

$$V_{z1} = [(1-V_C)V_y + V_C V_x] \cdot e^{-j\theta}, \tag{3a}$$

$$V_{z2} = [(1-V_C)V_x + V_C V_y] \cdot e^{-j\theta} \tag{3b}$$

$$V_x = A^2 e^{-j2\theta} V_{z1} \tag{4a}$$

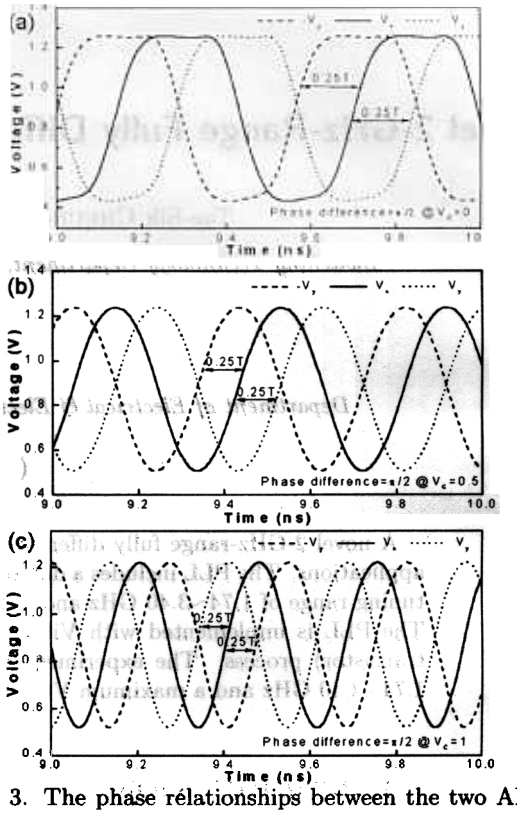

Fig. 3. The phase relationships between the two AMUX inputs when (a) V_C=0, (b) V_C=0.5, and (c) V_C=1.

$$V_y = A^2 e^{-j2\theta} V_{z2} \tag{4b}$$

In the above equations, A is the small signal gain of an inverter at a frequency of f_{OSC}, and θ is the output phase delay of an inverter and AMUX to its input signal. By using Eq. (3) and Eq. (4), we can obtain the relationship between V_{z1} and V_{z2} as

$$V_{z1} = \frac{(1-V_C)A^2 e^{-j3\theta}}{(1+V_C)A^2 e^{-j3\theta}} \cdot V_{z2}, \tag{5a}$$

$$V_{z2} = \frac{(1-V_C)A^2 e^{-j3\theta}}{(1+V_C)A^2 e^{-j3\theta}} \cdot V_{z1} \tag{5b}$$

By summing Eq. (5-a) and Eq. (5-b), we obtain the following equations:

$$\left[\frac{(1-V_C)A^2 e^{-j3\theta}}{+V_C A^2 e^{-j3\theta}}\right]^2 = -, \tag{6a}$$

$$\frac{(1-V_C)A^2 e^{-j3\theta}}{1+V_C A^2 e^{-j3\theta}} = \pm j. \tag{6b}$$

In Eq. (6-b), since the left term is the phase delay of V_{z1} on V_{z2} as shown in Eq. (5-b), "+j" in the right term is meaningless. Therefore, θ can be expressed in terms of A and V_C as

$$e^{-j3\theta} = \frac{-j}{A^2[(1-V_C)+jV_C}, \tag{7}$$

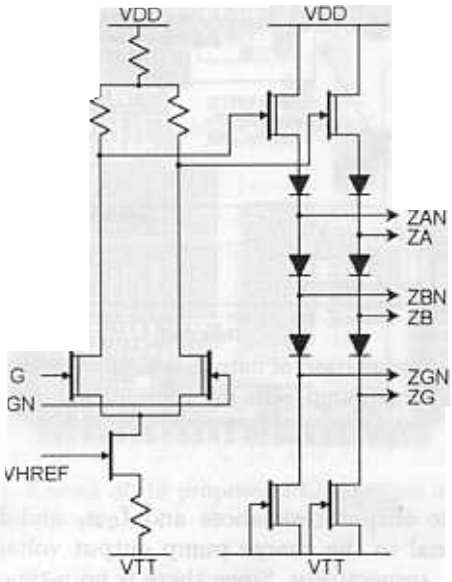

Fig. 4. Schematic diagram of the SCFL inverter

Also, θ can be expressed in terms of T_{OSC} and t_d as

$$\theta = \frac{2\pi t_d}{T_{OSC}}. \quad (8)$$

By combining Eq. (7) and Eq. (8), we can express $fosc$ as

$$fosc = \frac{\frac{\pi}{2} + \tan^{-1}\left(\frac{V_C}{1-V_C}\right)}{2\pi} \cdot \frac{1}{3t_d}. \quad (9)$$

From Eq. (9), it can be seen that the proposed VCO has a tuning range of $1/(12t_d)$~$1/(6t_d)$, which is wider than that of the conventional VCO structure shown in Fig. 1.

The advantage of the proposed VCO is that the AMUX input phase difference is fixed at $\pi/2$ over the entire tuning range. As shown in Fig. 2, the two inputs to AMUX1 and to AMUX2 are V_x and V_y and $-V_y$

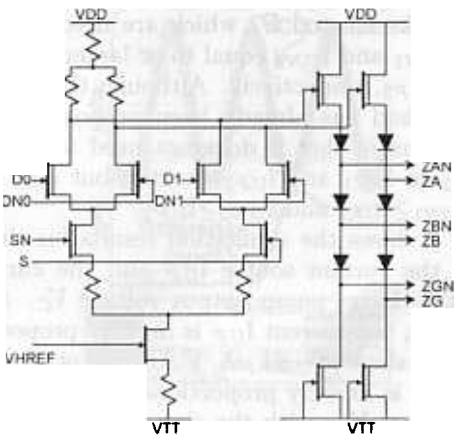

Fig. 5. Schematic diagram of the SCFL analog multiplexer.

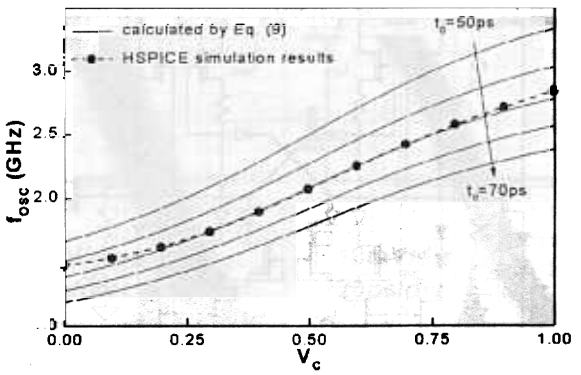

Fig. 6. Comparison of tuning sensitivity of the proposed VCO simulated by HSPICE with the result calculated using Eq. (9).

and V_x, respectively. In the case of AMUX1, the phase difference between V_y and V_x is exactly $\pi/2$ because V_y is the signal V_x delayed by $3t_d$, and V_x is an oscillating signal which has a period of $12t_d$. In case of AMUX2, the phase difference between V_x and $-V_y$ is also exactly $\pi/2$ because the phase difference between $-V_y$ and V_y is π.

Figure 3 shows the simulation results for the proposed VCO to evaluate the phase relationships of V_x, V_y, and $-V_y$ at V_C=0, 0.5, and 1. As shown in the figure, the phase differences between V_x and V_y and between V_x and $-V_y$ are exactly $\pi/2$ over the entire tuning range. This guarantees a stable operation of the AMUXs.

Figure 4 and Figure 5 show the schematic diagram of the SCFL(source-coupled field-effect transistor logic) inverter and SCFL AMUX used in the proposed VCO. Figure 6 shows both the HSPICE post-layout simulation results to evaluate the tuning sensitivity of the proposed VCO and the results calculated using Eq. (9) with various values of t_d. The simulation was performed at a temperature of 80 °C. From this, it can be seen that the simulated results are best fitted for t_d=60 ps and that the VCO tuning range is 1.48~2.84 GHz.

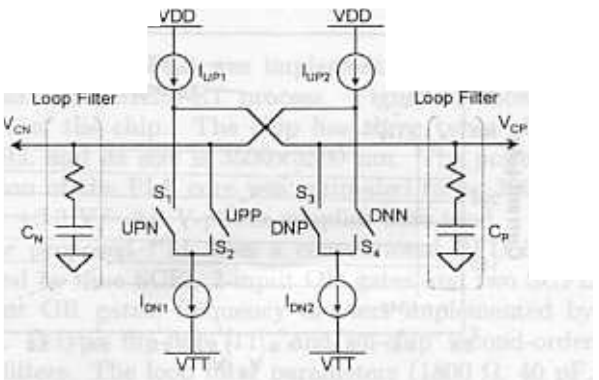

Fig. 7. Schematic diagram of the conventional charge pump.

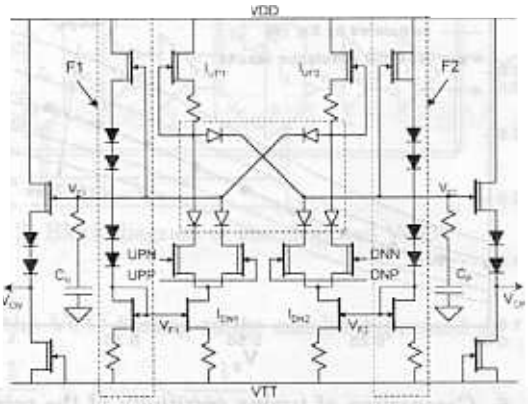

Fig. 8. Schematic diagram of the proposed charge pump

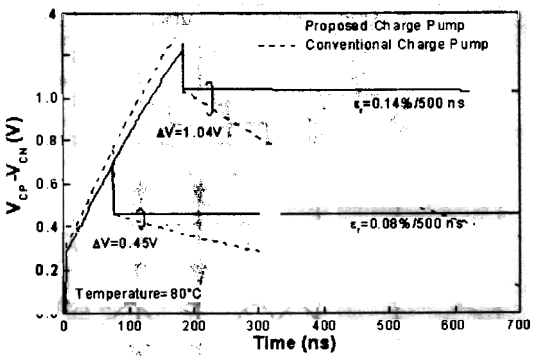

Fig. 10. Comparison of output hold characteristics of the proposed charge pump with the conventional one shown in Fig. 7.

III. CHARGE PUMP

1. Conventional Charge Pump

A differential charge pump is generally used for high-speed PLL applications because it switches only the current paths while the current sources and sinks are always turned on. Figure 7 shows a schematic diagram of a conventional differential charge pump [1]. In this figure, UPP, UPN, DNP, and DNN are the differential outputs of phase/frequency divider (PFD). When the charge pump is in the hold state (UP=DN="0"), I_{UP1} flows to I_{DN1} and I_{UP2} flows to I_{DN2}. If the currents I_{UP1} and I_{DN1}, and I_{UP2} and I_{DN2} are exactly the same, the charge pump outputs V_{CP} and V_{CN} are not changed. When the charge pump is in the up state (UP="1", DN="0"), I_{UP2} flows to I_{DN2}, I_{UP1} flows to the loop filter capacitor C_P making V_{CP} increased, and I_{DN1} flows from the loop filter capacitor C_N decreasing V_{CN}. In the same way, when the charge pump is in the down state (UP="0", DN="1"), V_{CP} is decreased and V_{CN} is increased.

However, as the charge pump output level is changed from its initial bias level, it tends to converge to its initial state because the current sources I_{UP1} and I_{UP2} have finite output resistances and I_{UP1} and I_{UP2} are proportional to the charge pump output voltages V_{CP} and V_{CN}, respectively. Since there is no p-type FET in the GaAs MESFET process, it is very difficult to design proper current sources. Consequently, this problem is more serious than it is with the CMOS process.

In Ref. 9, a differential charge pump was proposed to minimize this problem by controlling I_{DN1} and I_{DN2} with the charge pump outputs. However, the above problem cannot be solved completely, because it is very difficult to match I_{DN1} and I_{DN2} to I_{UP1} and I_{UP2} exactly.

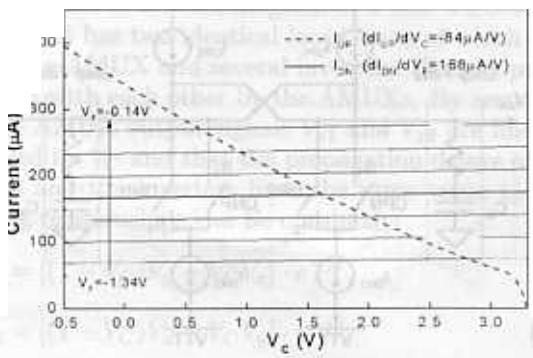

Fig. 9. The dependence of the currents I_{UP} and I_{DN} on V_C and V_F.

2. Proposed Charge Pump

Figure 8 shows a schematic diagram of the proposed charge pump [10]. In order to increase the output resistance of all current sources and sinks, we implement them by a cascode structure using one GaAs MESFET and one resistor. Six enhancement mode GaAs MESFET diodes are placed in all the current paths to prevent the charges in the loop filter capacitors from flowing to the current sinks I_{DN1} and I_{DN2} at the hold state. Also, the leakage currents from the current sources I_{UP1} and I_{UP2} to C_P and C_N can be blocked by the current sink control blocks F1 and F2 which are used to make the currents I_{DN1} and I_{DN2} equal to or larger than those of I_{UP1} and I_{UP2}, respectively. Although the current sink control method has already been proposed in [9], our scheme differs in that it does not need to match I_{DN1} and I_{DN2} to I_{UP1} and I_{UP2} exactly, but only needs to satisfy $I_{DN1} \geq I_{UP1}$ and $I_{DN2} \geq I_{UP2}$.

Figure 9 shows the simulation results for the dependence of the current source I_{UP} and the current sink I_{DN} on the charge pump output voltage V_C. As shown in the figure, the current I_{UP} is linearly proportional to V_C with the slope of -84 μA/V. On the other hand, the current I_{DN} is linearly proportional to the current sink control voltage V_F, with the slope of 168 μA/V, but it is nearly independent of V_C. From this, it can be seen that the current sink control block F1 and F2 must have

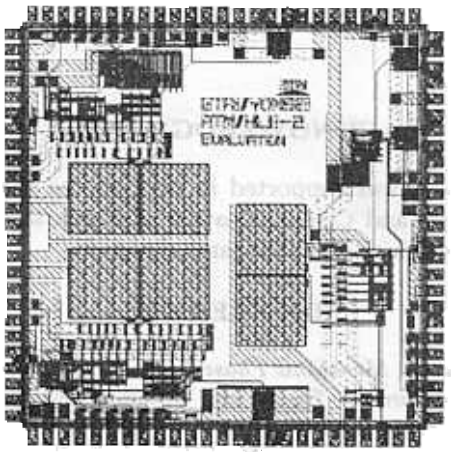

Fig. 11. Layout of the proposed PLL (3-types of PLLs are included in the chip).

a voltage gain, dV_F/dV_C, larger than 0.5 to satisfy the relationship $I_{DN} \geq I_{UP}$. Therefore, a source follower with the small signal gain of 1 can be used for F1 and F2.

Figure 10 shows the simulation results for the output hold characteristics of the proposed charge pump and

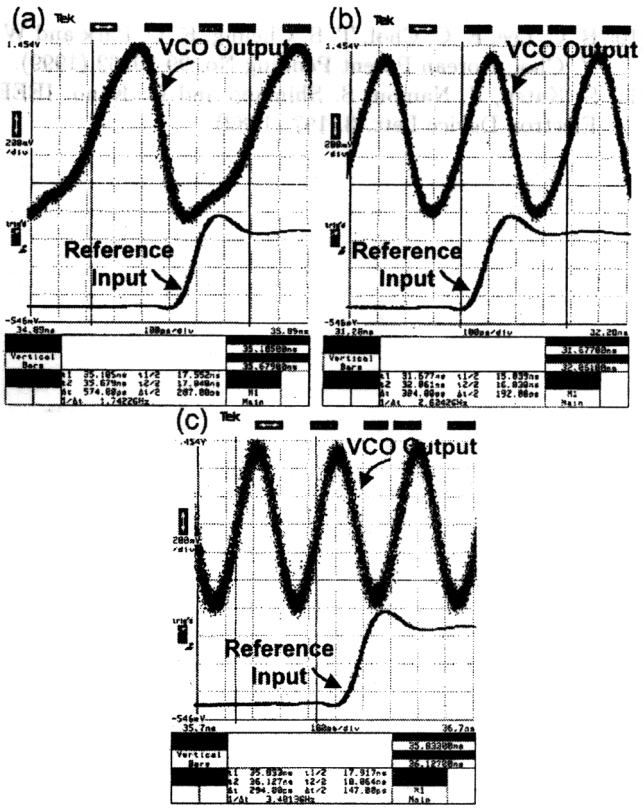

Fig. 12. Waveforms of the input reference signals and VCO outputs when the proposed PLL is locked at (a) 1.74 GHz, (b) 2.60 GHz and (c) 3.40 GHz.

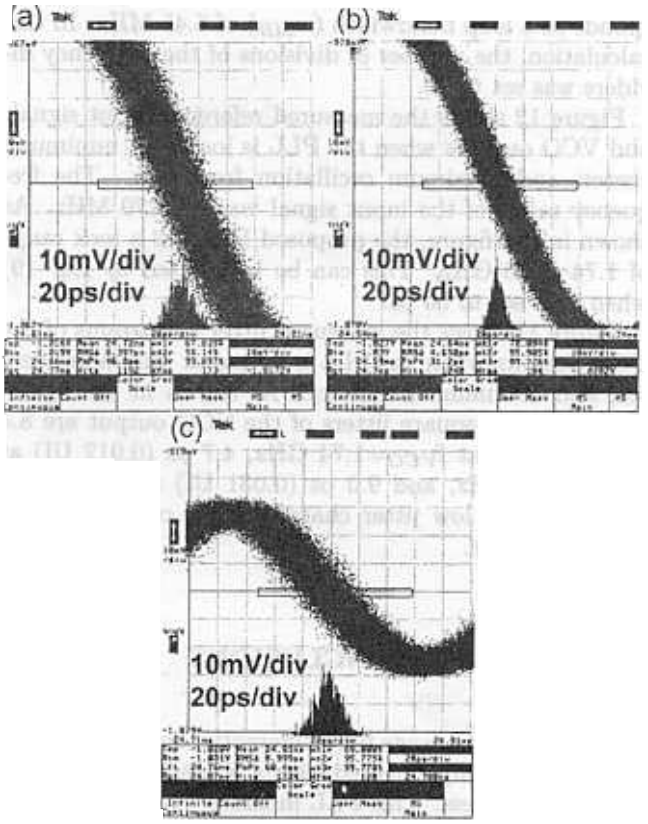

Fig. 13. Measured jitter histogram of the VCO output when the PLL is locked at (a) 1.74 GHz, (b) 2.60 GHz and (c) 3.40 GHz.

the conventional one. The conventional charge pump tends to converge to its initial state as the output level goes up from its initial bias level. On the other hand, the proposed charge pump's output level stays at the hold state. The maximum relative error of the proposed charge pump output is 0.14 % during 500 ns, showing output hold characteristics which are superior to those of the conventional charge pump.

IV. EXPERIMENTAL RESULTS

The proposed PLL was implemented with a Vitesse 0.5-μm GaAs MESFET process. Figure 11 shows the layout of the chip. The chip has three types of PLL circuits, and its size is 3500×3500 μm. The power dissipation of the PLL core was estimated to be 380 mW when +3.3 V/−2.0 V power supplies were used.

The proposed PLL uses a conventional PFD implemented by nine SCFL 2-input OR gates and two SCFL 3-input OR gates, frequency dividers implemented by SCFL D-type flip-flop [11], and on-chip second-order loop filters. The loop filter parameters (1800 Ω, 40 pF, and 4 pF) were chosen to make the damping factor (ζ) of the closed-loop transfer function 0.707, which corre-

sponds to a loop bandwidth (ω_{3dB}) of 6.45 MHz. In this calculation, the number of divisions of the frequency dividers was set to 20.

Figure 12 shows the measured reference input signals and VCO outputs when the PLL is locked at minimum, center, and maximum oscillation frequency. The frequency range of the input signal was 87~170 MHz. As shown in the figure, the proposed PLL has a lock range of 1.74~3.40 GHz. This can be best fitted by Eq. (9) when t_d is set to 50 ps.

Figure 13 shows the measured jitter histograms of the VCO outputs when the PLL is locked at minimum, center, and maximum frequency. As shown in the figure, the root-mean-square jitters of the VCO output are 8.4 ps (0.015 UI) at f_{VCO}=1.74 GHz, 4.7 ps (0.012 UI) at f_{VCO}=2.60 GHz, and 9.0 ps (0.031 UI) at f_{VCO}=3.40 GHz, showing low jitter characteristics over the entire PLL lock range.

V. CONCLUSIONS

A novel 2-GHz-range fully differential on-chip PLL was proposed and implemented with a Vitesse 0.5-μm GaAs MESFET process. This PLL includes a newly proposed VCO which has an enhanced tuning range and stability, and a newly proposed differential charge pump which has improved output hold characteristics. The experimental results show that the proposed PLL has a lock range of 1.74~3.40 GHz and the maximum root-mean-square jitter of 9.0 ps (0.031 UI). It is believed that the proposed PLL can be very useful for high-speed clock-generating systems.

ACKNOWLEDGMENTS

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