

A Novel 2GHz-Range Fully Differential GaAs MESFET Phase-Locked Loops

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Introduction: In multi-link systems such as ATM system, it is more cost-effective to integrate several links into one high-speed link because it can reduce the system complexity. This requires high-speed phase-locked loops(PLLs) which provide the synthesized system clock for data serialization and deserialization[1].

In this paper, a 2GHz-range fully differential 0.5 μ m GaAs MESFET PLL is proposed for ATM clock generation applications. This PLL has a differentially controlled VCO with wide tuning range and a charge pump with improved hold characteristics.

VCO: Figure 1 shows the block diagram of the proposed VCO. This combines two identical 3-stage ring oscillators, and each oscillator is made up of one analog MUX and two SCFL inverters[2]. The proposed VCO can overcome the MUX operation instability and tuning range limitation found in previously reported VCO with analog MUX.

Assuming that the analog MUX linearly combines two inputs, VCO oscillation frequency(f_{osc}) can be expressed as

$$f_{osc} = \frac{\frac{\pi}{2} + \tan^{-1}\left(\frac{C}{1-C}\right)}{2\pi} \cdot \frac{1}{3t_d} \quad (1)$$

where, C ($0 \leq C \leq 1$) is the mixing ratio of the analog MUX, and t_d is the propagation delay of analog MUX and SCFL inverter. By varying C from 0 to 1, f_{osc} can be tuned from $1/12t_d$ to $1/6t_d$. Figure 2 shows the HSPICE simulation results and the calculated results for f_{osc} . According to the simulation results, the VCO has the tuning range of 1.48GHz ~ 2.84GHz and gain of 1.35GHz/V.

Charge Pump: In order to make the PLL lock-range wider, a charge pump must have highly stable output hold characteristics at any output levels[3]. A new charge pump is proposed[4], which overcomes current mismatch problems of conventional charge pumps by use of GaAs MESFET diodes and a feedback scheme as shown in Figure 3.

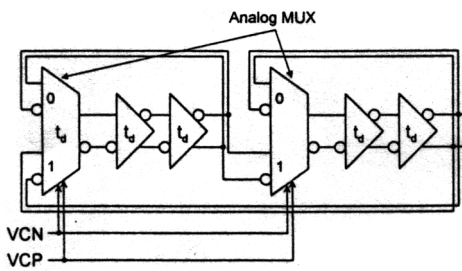
Figure 3 shows the schematic diagram of proposed charge pump with loop filters. 40pF of on-chip capacitors and 1150 Ω of N⁺ resistors are used for the loop filter and the charge pump output currents are 150 μ A. The charge pump has 6 enhancement mode MESFET diodes and feedback circuits.

The feedback circuits(F1, F2) are designed to overcompensate I_{DN1} and I_{DN2} so that they are equal or larger than I_{UP1} and I_{UP2} , respectively. This prevents the loop filters from being charged by I_{UP1} and I_{UP2} at hold state. Diodes D_1 and D_2 prevent the loop filters being discharged by I_{DN1} and I_{DN2} at hold state. With these, the hold characteristics of the proposed charge pump are enhanced. Figure 4 shows the HSPICE simulation results to compare the hold characteristics of the proposed charge pump with the conventional one without any compensation scheme. Simulation is performed by applying UP signals for 70ns and 200ns, and measuring the charge pump output levels at hold state. At the highest output level, the relative error of VCP-VCN is 0.14% for the duration of 500ns indicating high stability.

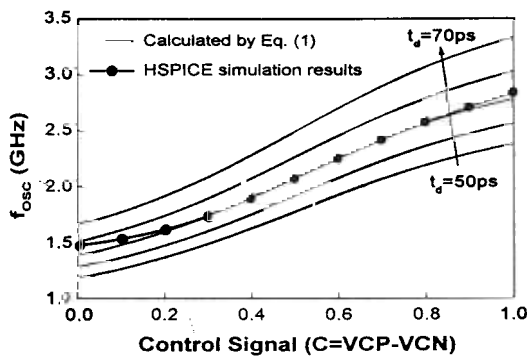
Simulation Results and Discussion: The proposed PLL was implemented with 0.5 μ m GaAs MESFET and evaluated by post-layout simulation using HSPICE. Conventional PFD and frequency divider(1/8) were used[1]. Figure 5 shows the layout of the proposed PLL. Loop filter(1150 Ω , 40pF) is designed to make damping factor(ζ) of the closed-loop transfer function to be 0.707, which corresponds to loop bandwidth(ω_{3dB}) of 1.04MHz in our circuit. Figure 6 and Figure 7 show the simulation results for the pull-in process characteristics, static phase error(θ_v), and VCO jitter of the proposed PLL. The operation temperature is set to 80°C and +3.3V/-2.0V of power supplies are used. According to the simulation results, the proposed PLL has the lock-range of 1.6GHz ~ 2.5GHz, the $\theta_{v,max}$ of 7.88°, and the maximum VCO peak-to-peak jitter of 0.82ps (0.0016UI). It is currently being fabricated, and the experimental results will be presented.

References:

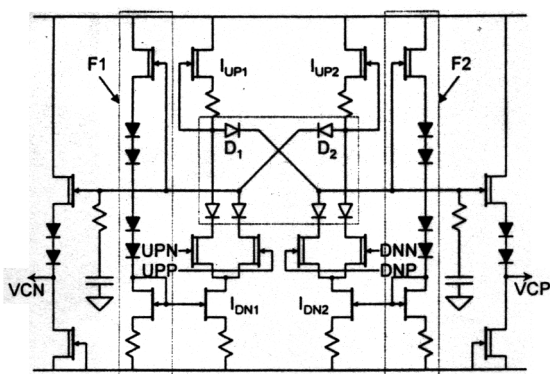
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- [2] R.C. Walker, "Fully integrated high-speed voltage-controlled ring oscillator," U.S. Patent, 4884041, 1989.
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- [4] B.C. Lee, E.C. Choi, T.S. Cheung, and W.Y. Choi, "High speed differential charge pump circuit," Korean Patent, Application Number: 99-29262, 1999.



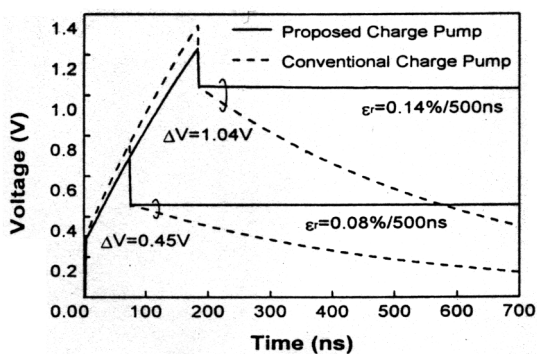
[Figure 1] Block Diagram of proposed VCO.



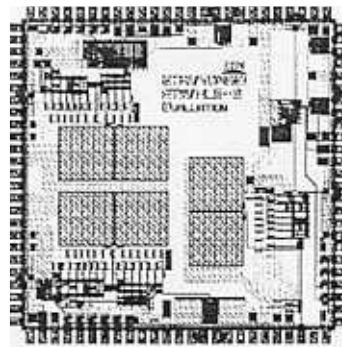
[Figure 2] Tuning sensitivity of the proposed VCO.



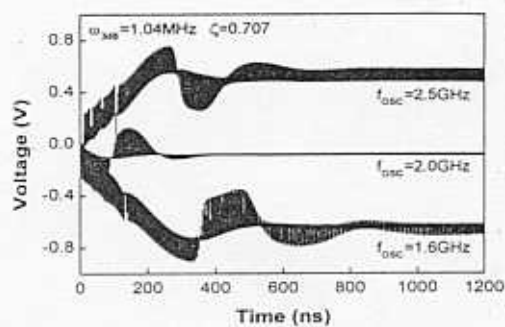
[Figure 3] Schematic diagram of proposed charge pump.



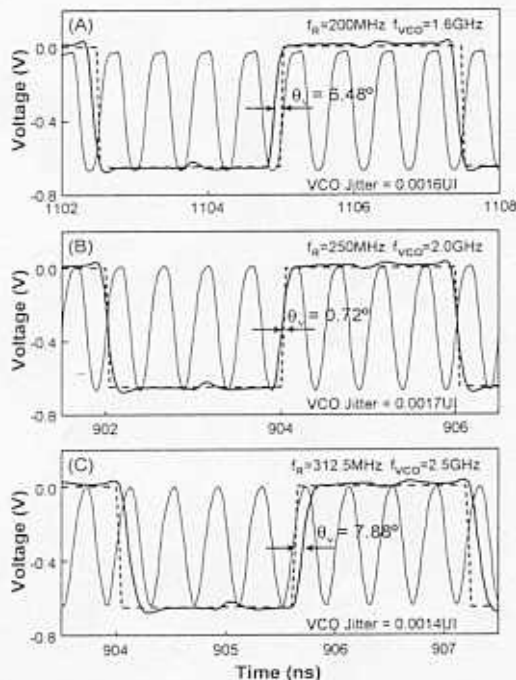
[Figure 4] Hold characteristics of the proposed charge pump.



[Figure 6] Layout of the proposed PLL. (3750nm × 3750nm) (3-types of PLL's are included in the chip)



[Figure 7] Pull-in process characteristics of the proposed PLL.



[Figure 7] Simulation results to evaluate θ_o and VCO jitter. (bold solid line: reference input signal, bold dashed line: divided VCO output, thin solid line: VCO output)