2006 International SoC Design Conference

COEX Conference Center, Seoul, Korea
26~27 October, 2006



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International
SoC Design Conference

13:00 ~ 13:20

- DTMW : Duplicated Transition Monitoring Window for Low Power Test based on Pseudo-Random BIST

Youbean Kim, Dongsup Song, Kicheol Kim, Incheol Kim, Sungho Kang, Yonsei Universiry

13:20 ~ 13:40

- A New Low Power Scan Architecture Considering Test Data Compression

Hong-Sik Kim, Beom Ik Cheon, Kyu-Myoung Choi, Jeong-Taek Kong, Samsung Electronics

13:40 ~ 14:00

- TRACE : Transition Repression Architecture for low power scan CEII in BIST environment

Incheol Kim, Dongsup Song, Kicheol Kim, Youbean Kim, Sungho Kang, Yonsei University

14:00 ~ 14:20

- A New BIST Architecture for Word oriented Memory

Il-Woong Kim, Gunbae Kim, IlgWeon Kang, Sungho Kang, Yonsei University

14:20 ~ 14:40

- A Functional Pattern Generation Method For Faulty Scan Chain Diagnosis

Mingyu Sim, Sungho Kang, Yonsei University

14:40 ~ 15:00 Coffee Break

15:00 ~ 16:30 Tutorial II [Room 311]

Session Chair :
Shin-Il Lim (Seokyeong University)

Signal Integrity : Overview

Hong-June Park (Professor, POSTECH, Korea)

15:00 ~ 16:40 Session 5 [Room 321A]

Analog and Mixed-Signal Circuit II

Session Chair :
Jong Kug Seon (LS Industrial Systems)
Yeong-Seuk Kim (Chungbuk National University)

15:00 ~ 15:20

- A Design of Full-CMOS Single-Chip PHY IC for Power Line Communication(PLC) Systems

YoungGun Pu, Kang-Yoon Lee, KonKuk University

15:20 ~ 15:40

- A Novel BPSK Demodulating Scheme Using a Half-rate Bang-bang Phase Detector

Duho Kim, Woo-young Choi, Young-kwang Seo*, Hyunchin Kim*, Yonsei University, *Samsung Electronics

15:40 ~ 16:00

- A Synchronous, Self-Oscillating, Fully Integrated CMOS DC-DC Converter with a New Adaptive Mode-Switching Mechanism

Sau-Mou Wu, Chung-Lin Wu, Yuan Ze University

16:00 ~ 16:20

- A 80% Efficiency Digital Audio Amplifier with 4-Ω Speaker Load Using 1-bit 4th-order Delta-Sigma Modulation

Kyoungsik Kang, Youngkil Choi, Hyungdong Roh, Sanho Byun, Hyuntae Lee, Jeongjin Roh, Hanyang University

16:20 ~ 16:40

- Formal Specification and Analysis of Analog and Mixed-Signal Circuits Using Process Algebras for Hybrid Systems (with a focus on hybrid process algebra ACP^srt_hs)

K.L.Man, M.P. Schellekens, M. Boubekeur, The Center of Efficienty-Oriented Languages (CEOL)

15:00 ~ 16:40 Session 6 [Room 321B]

Display Driver and Imaging Devices I

Session Chair :
Byong-Deok Choi (Hanyang University)
Taesung Kim (Samsung Electronics)

A Novel BPSK Demodulating Scheme

Using a Half-rate Bang-bang Phase Detector

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Abstract – *The Costas-loop is commonly used in BPSK demodulation. But it is very difficulty to implement the low-pass-filter for a high frequency carrier. This paper analyzes the Costas-loop as a phase-tracking-architecture and proposes a new BPSK demodulation scheme that uses a half-rate bang-bang phase-detector.*

Keywords: BPSK, tracking, Costas-loop, half-rate bang-bang PD,

1 Introduction

There are many electronic appliances at home and there is an increasing demand for establishing communication among them. Since installing new lines for linking home appliances at home causes many problems, approaches based on either wireless communications or already-built-in lines are preferred.

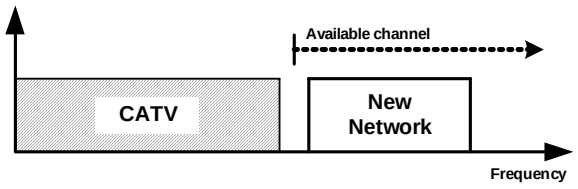

Figure 1. Channel use of cable line

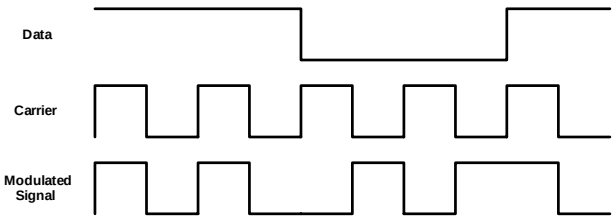

Figure 2. BPSK modulation

In the second approach, using cable lines installed in many houses is one good solution. In order to establish new home-networking communication channels based on cable lines, high-frequency carriers have to be used so that cable TV signals are not affected as shown in figure 1. In addition, the new home-networking communication must support very high data rates since many of today's home applications demand high data rates.

The goal of our research is realizing a high-speed BPSK modem with a high carrier frequency (> GHz) that can be used for the above-mentioned application. We are interested in BPSK because its modulation scheme is simple as shown in figure 2 and, because of that, it is possible to realize a modem with GHz-range carrier frequency. In this paper, we first analyze the Costas-loop, the classic BPSK demodulator scheme, identify its problems for our application, and proposes a novel scheme which overcomes such problems.

2 Costas Loop

Figure 3 shows the block diagram of the Costas-loop. At first, two sine waves with 90-degree phase difference are multiplied to the modulated signal. Assume that Θ is the phase difference between transmitter and receiver carries, two outputs of multipliers are given as

$$m(t)\cos(\omega t)\cos(\omega t+\theta) = m(t)\{\cos\theta+\cos(2\omega t+\theta)\}/2$$

$$m(t)\cos(\omega t)\sin(\omega t+\theta) = m(t)\{\sin\theta+\sin(2\omega t+\theta)\}/2$$

The LPF removes high frequency terms having 2ω, so that only the terms having θ remain. Then, the product of two LPF outputs is given as

$$m(t)^2\cos\theta\ \sin\theta$$

which is proportional to the square of m(t). But this square term is always 1 because m(t) is either '1' or '-1'. So we can get the output of $\sin 2\theta$. The phase difference will disappear with the feedback-loop which makes θ zero.

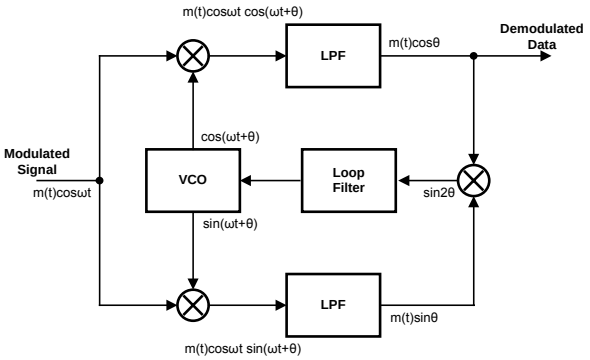

Figure 3. Block diagram of a Costas-loop

In addition, m(t) is also recovered when the phase difference goes to zero, because outputs of two LPFs are m(t)cosθ and m(t)sinθ.

However, it is difficult to implement the LPF for very high frequency carriers. By using a simple RC structure, the flatness of the high frequency response is poor. The required area for the filter is also large. With these problems, the circuit cannot be used for high-frequency applications.

3 Novel Structure

The Costas-loop is a phase-tracking architecture like CDR or PLL. Mixers and LPFs in the conventional structure can be simplified as a PD(phase detector) having the output of sin2θ as shown in figure 4. The characteristics of this PD are shown in figure 5. It is similar to the characteristics of the commonly used half-rate PD in CDRs, shown in figure 6.

It is possible to demodulate the BPSK signal by using a half-rate bang-bang PD as shown in figure 7. The shape of the BPSK signal is similar to "1010" when the data is high and "0101" when the data is low. By using the half-rate bang-bang PD, the clock of the receiver can synchronize the modulated signal and sample the data sequence as "1010…0101". After inverting the data sampled at the falling edge, the transmitted data are recovered.

Because of the frequency offset between data and the carrier, transitions at wrong timing can occur at the transition of data. But there are more transitions at correct timing if the data rate is sufficiently lower than the carrier frequency.

The block diagram of the proposed demodulator is shown in figure 8. An LPF is added to reject jitters from sampling. But in this scheme, a digital filter can be used because the input signal is oversampled. Using a digital filter significantly decreases the cost of circuit realization.

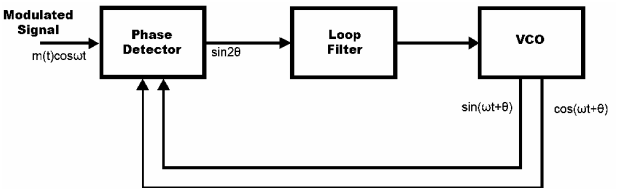

Figure 4. Modified block diagram of a Costas-loop

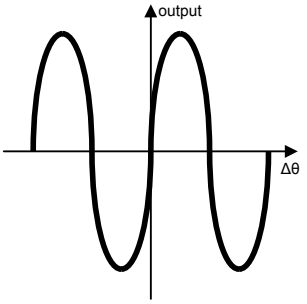

Figure 5. Characteristic of Costas-loop as a PD

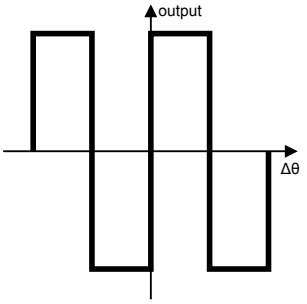

Figure 6. Characteristic of half-rate bang-bang PD

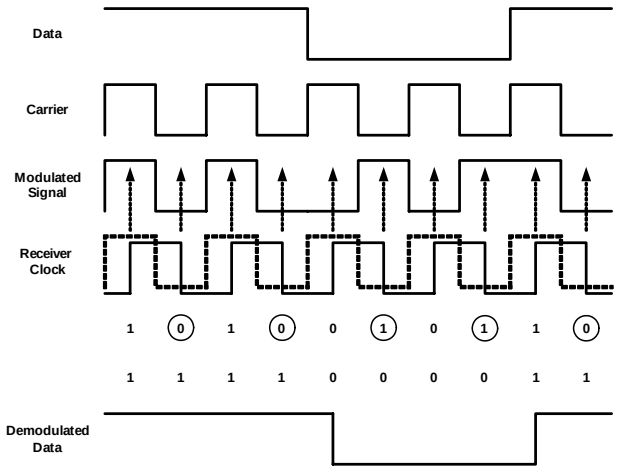

Figure 7. Proposed demodulating scheme

The additional CDR after the demodulator can be implemented easily by using an oversampling CDR architecture such as [1].

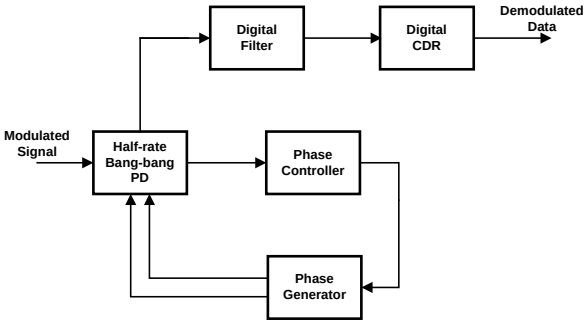

Figure 8. Block diagram of the proposed demodulator

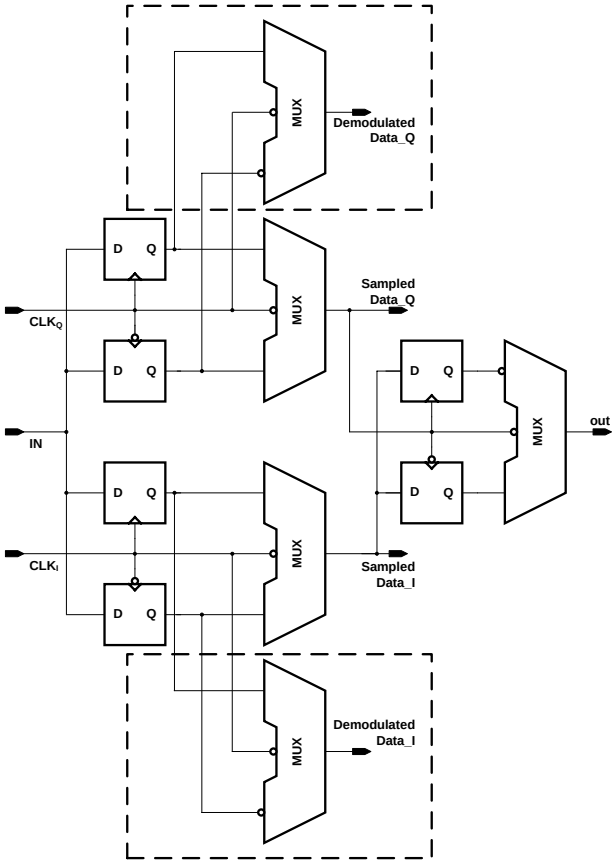

Figure 9. Modified half-rate bang-bang PD

BPSK demodulator can use any type of CDR architectures by using a half-rate PD. We can also use any type of half-rate PDs and phase control algorithms.

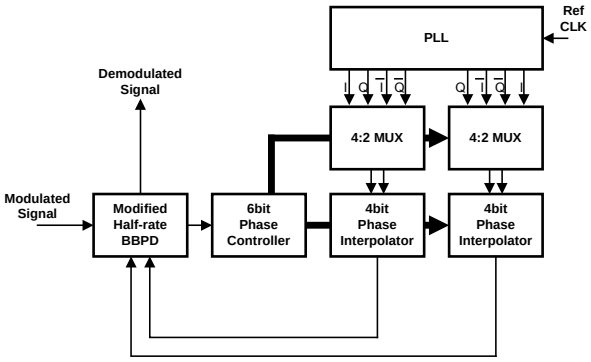

Figure 10. Block diagram of the test demodulator

4 Implementation

In order to implement the desired PD, the PD shown in [2] is modified as shown in figure 9. Two multiplexers inside the dotted line are added. They invert the sample at the falling edge of the clock. So the modified PD outputs the phase information and also demodulated data.

This PD outputs only two states, lead or lag. In CDR applications, it can cause a problem in that the 2-state PD produces a wrong state output when there is no transition. But in BPSK applications, it does not matter if the data rate is sufficiently lower than the carrier frequency, because the wrong state output appears only at the transition of data.

To verify the operation of our scheme, we designed a test circuit by using TSMC 0.18 μm process. This test circuit uses the phase control algorithm given in [3]. But the test circuit has two interpolators using the same controller and different phases from PLL as shown in figure 10, because the half-rate PD needs multi-phase clocks.

5 Simulation Results

The target carrier frequency is 2.5GHz and the target data rate is 500Mb/s. Since it is impossible to achieve perfect frequency match between transmitters and receivers, we added +0.02% frequency offset to the reference clock of the receiver in our simulation. The frequency offset between the carrier and data is not considered so that the eye diagram of modulated signals can be observed.

Figure 11 shows the HSPICE simulated eye-diagram showing the data sampling points. The gray line is the sampling clock in the demodulator. The BPSK-modulated

signals have similar eye-diagrams to the eye-diagram of the data sequence. The sampling clock is centered. The peak-to-peak jitter is 34.255ps in this simulation. Figure 12 shows demodulation process.

6 Conclusions

We analyzed the conventional Costas-loop structure with a different perspective, and came up with a novel scheme to demodulate BPSK signals. This demodulator can handle a very high carrier frequency such as 2.5GHz. The demodulator was designed with TSMC 0.18μm CMOS process, and the simulation was done for demodulating 500Mb/s data with 2.5GHz carrier frequency. Simulation results show that the proposed scheme can be used for the demodulation of BPSK signal modulated with high frequency carrier.

References

[1] S. Kim et al., "An 800Mb/s Multi-channel CMOS Serial Link with 3× Oversampling", *Proc. Of the IEEE Custom Integrated Circuits Conference*, pp. 451–54, May 1995.

[2] Ansgar Pottbacker, Ulrich Langmann and Hans-Ulrich Schreiber, "A Si Bipolar Phase and Frequency Detector IC for Clock Extraction up to 8 Gb/s", *JSSC*, Vol 27, No. 12, pp. 1683-1692, Dec. 1992.

[3] Stefanos Sidiropoulos and Mark A. Horowitz, "A Semidigital Dual Delay-Locked Loop", *JSSC*, Vol 37, No. 11, pp. 1683-1692, Nov. 1997.

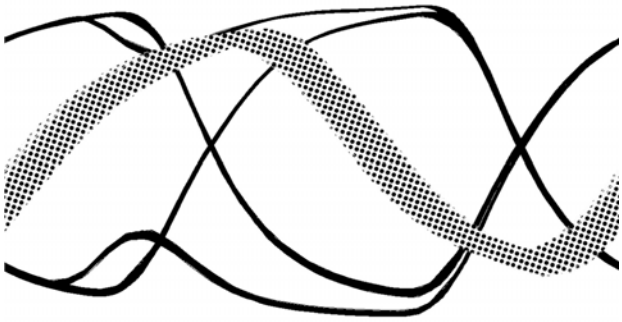

Figure 11. Simulation result : Sampling

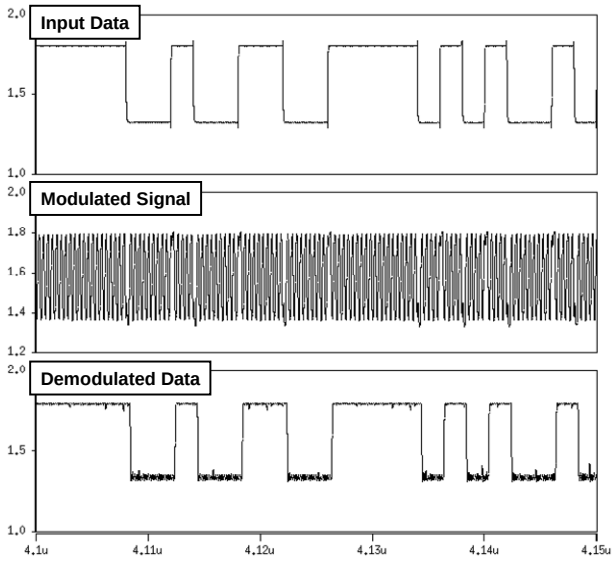

Figure 12. Simulation result : Demodulation