November 14, 2007 (Wed.)

[MSP2] Mixed-Signal Circuits for Communications
Time: 14:10-16:15 Room: Room 1 (Ramada Ballroom 1)
Session Co-Chairs: Kazutami Arimoto (Renesas, Japan) Oh-Kyung Kwon (Hanyang Univ., Korea)

14:10-14:35	**MSP2-1**	**A 2.5V, 5mW UMTS and GSM Dual Mode Decimation Filter for Sigma Delta ADC** *Chi Zhang (Carinthia Univ. of Applied Sciences, Austria)*
14:35-15:00	**MSP2-2**	**An Anti-Harmonic, Programmable DLL-Based Frequency Multiplier for Dynamic Frequency Scaling** *Jabeom Koo (Korea Univ., Korea)*
15:00-15:25	**MSP2-3**	**An Optimal Design of High Performance Interface Circuit with Acoustic Transducer Model** *Yu-Chun Hsu (Industrial Tech. Research Inst., Taiwan)*
15:25-15:37	**MSP2-4**	**A High-Speed Low-Complexity Two-Parallel Radix-24 FFT/IFFT Processor for UWB Applications** *Hanho Lee (Inha Univ., Korea)*
15:38-16:03	**MSP2-5**	**A 622Mb/s BPSK Demodulator with Mixed-mode Demodulation Scheme** *Duho Kim (Yonsei Univ., Korea)*
16:03-16:15	**MSP2-6**	**A Low Power Baseband OFDM Receiver IC for Fixed WiMAX Communication** *Jen-Ming Wu (National Tsing Hua Univ., Taiwan)*

A 622Mb/s BPSK Demodulator with Mixed-mode Demodulation Scheme

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***Abstract*- A new mixed-mode binary phase shift keying (BPSK) demodulator is demonstrated using a half-rate bang-bang phase detector commonly used in clock and data recovery (CDR) applications. This demodulator can be used for new home networking applications based on cable TV lines. A proto-type chip is realized that can demodulate up to 622Mb/s data at 1.4GHz carrier frequency.**

I. INTRODUCTION

There are many A/V appliances at home such as DVD players, HDTV, and satellite receivers, and establishing communication among these appliances is an important market demand. However, installing new lines for linking home appliances at home is not an easy task and, consequently, approaches using either wireless channels or already-built-in wirelines are preferred. For the second approach, using cable TV (CATV) lines that are already installed in many houses can be an attractive solution. Fig. 1(a) schematically shows such an approach. A switching hub and RF combiners are inside the wall with a CATV splitter. The switching hub connects a set-top box to many display terminals in several locations.

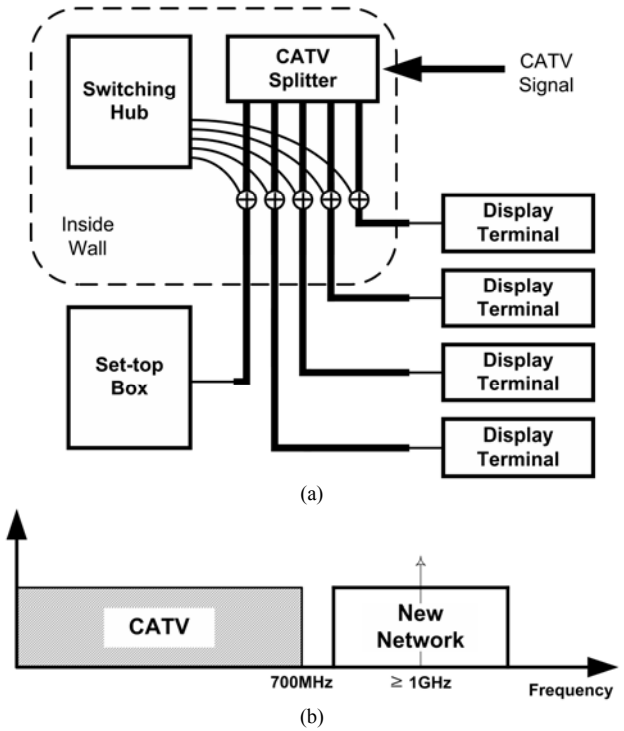

Fig. 1. CATV line network (a) block diagram (b) channel assignment

In order to establish communication channels based on CATV lines, high-frequency carriers above 1GHz must be used so that CATV signals(≤700MHz) are not disturbed by the A/V data streams as can be seen in Fig. 1(b). BPSK MODEM chips that satisfy this requirement are not easily available. Although such modulation techniques as QPSK and QAM are preferred since they utilize bandwidth more efficiently, we tried BPSK first because it is simpler and more suitable for the initial trial.

There are several types of BPSK demodulators. In the analog approach, the carrier signal can be recovered by using a phase-locked loop (PLL) after the received signal is squared [1]. With this scheme, the phase error between the received signal and the recovered carrier signal remains. Costas-loop [2] is another classical analog approach and will be analyzed in the later part of this paper. In the digital approach, several different architectures are possible depending on ADC configuration [3], but the maximum data rate is limited by the speed of ADC. Digital interpolation schemes [4] [5], which is the most popular digital approach, need GSamples/s ADC to oversample hundreds of Mb/s data, and its realization with CMOS is difficult. In this paper, we report a new mixed-mode BPSK demodulator with a 1.4GHz carrier frequency that can be used for above-mentioned applications. Our demodulator is based on CMOS so that one-chip solution including all the digital functions is possible.

This paper is organized as follows. Section II analyzes the classical analog BPSK demodulator based on Costas-loop and introduces the new mixed-mode demodulation scheme. Section III describes the implementation of the proto-type chip. Section IV gives measurement results of the fabricated chip as well as its link performance.

II. COSTAS LOOP

Fig. 2 is the block diagram of the Costas-loop. Two sine waves with 90-degree phase difference are multiplied to the modulated signal. Assume that θ_e is the phase difference between carriers for the transmitter and receiver, two outputs are given as:

$$m(t)\cos(\omega t)\cos(\omega t+\theta_e) = m(t)\{\cos\theta_e + \cos(2\omega t+\theta_e)\}/2$$
$$m(t)\cos(\omega t)\sin(\omega t+\theta_e) = m(t)\{\sin\theta_e + \sin(2\omega t+\theta_e)\}/2 \quad (1)$$

Low pass filters (LPFs) remove high frequency terms having 2ω, so that only the terms having θ_e remain. The

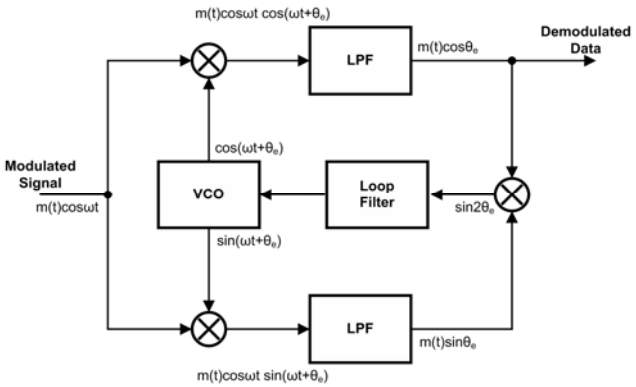

Fig. 2. Block diagram of a costas-loop

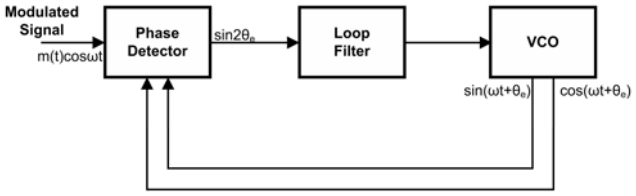

Fig. 3. Modified block diagram of a costas-loop

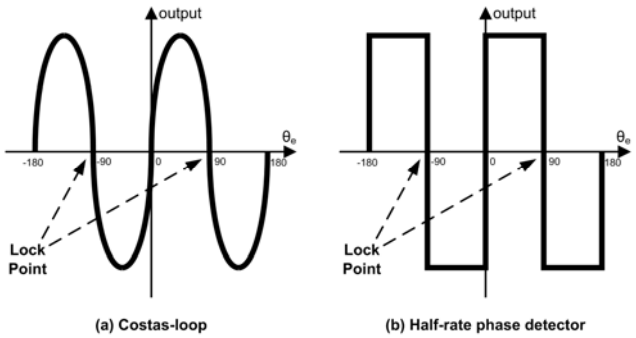

Fig. 4. Phase detection characteristic of costas-loop & half-rate bang-bang PD

product of two LPF outputs results in terms having square of m(t), which is always 1 since m(t) is either 1 or -1. Consequently the output becomes $\sin 2\theta_e$. The phase difference will disappear by using the feedback-loop to make θ_e zero and m(t) is recovered.

When realizing Costas-loop for high frequency carrier applications, it is difficult to implement LPFs. By using a simple RC filter, flatness of pass-band response and sharpness of cutoff band are poor. A large area is also needed due to capacitors. Although, better flatness and sharpness can be achievable with other filter types, they usually need more chip areas. We solve these problems with a new mixed-mode BPSK demodulator.

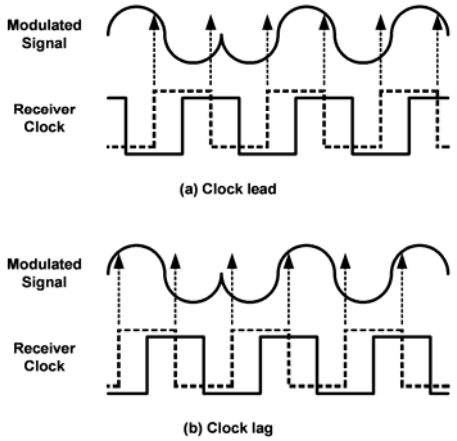

Fig. 5. Tracking BPSK signal by half-rate bang-bang PD

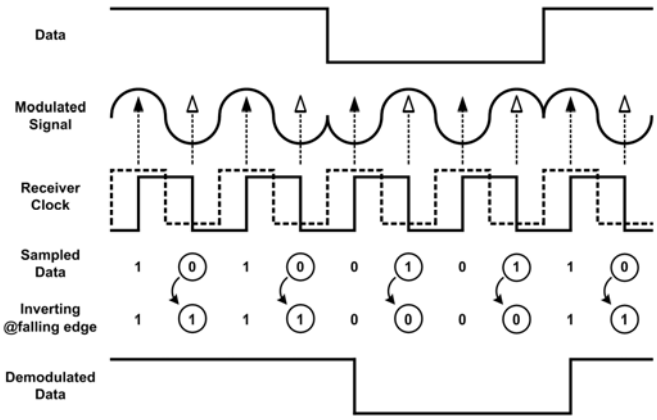

Fig. 6. Proposed demodulation scheme

The phase-tracking characteristics of Costas-loop can be represented by a block diagram shown in Fig. 3. Here, one phase detector block represents the functions performed by three mixers and two LPFs in Fig. 2. In this block diagram, the phase detector (PD) takes modulated signals and two clocks having 90-degree phase difference as input and produces $\sin 2\theta_e$ as output.

Then the phase detecting characteristics of Costas-loop can be represented as shown in Fig. 4(a). Because BPSK signal changes its phase by 180˚, this curve has two lock points separated by 180˚. Similar PD characteristics can be realized with a half-rate bang-bang PD, commonly used for CDR applications, as shown in Fig. 4(b).

Fig. 5 shows how a half-rate bang-bang PD tracks BPSK signal. The dotted line is the tracking clock and the solid line is the sampling clock. The tracking clock tracks transition edges of input signal. If the tracking clock leads the modulated signal, the phase adjustment circuit makes its

clock slower and if it lags, the phase adjustment circuit makes its clock faster.

After synchronization, edges of the sampling clock are aligned to centers of input signal as shown in Fig. 6. In the figure, arrows indicate sampling points of PD. Black arrows are rising edges and white arrows are falling edges of the sampling clock. Then the bang-bang PD produces output sequence which consists of 10 and 01. BPSK demodulation is done by making decision for high when the sequence is 10, and low when the sequence is 01. This can be easily realized by inverting samples at falling edges of the sampling clock, so that the 10 sequence becomes 11, and the 01 sequence 00. This BPSK demodulation scheme can use any type of CDR architectures using a half-rate PD.

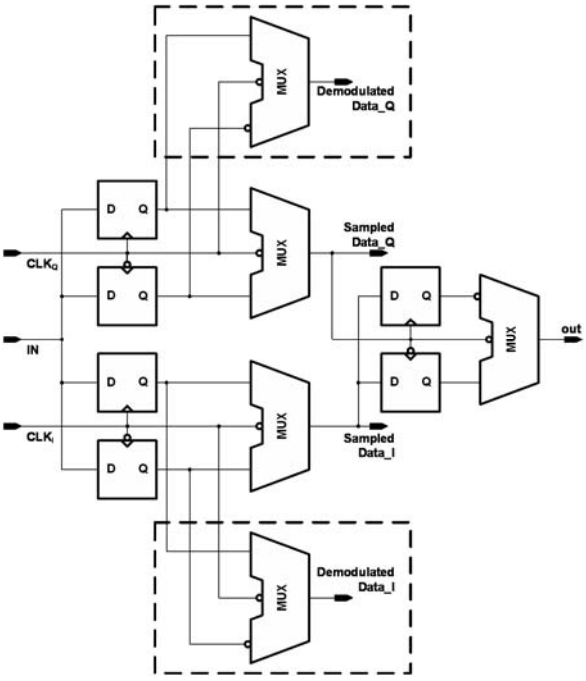

Fig. 7. Modified half-rate bang-bang PD

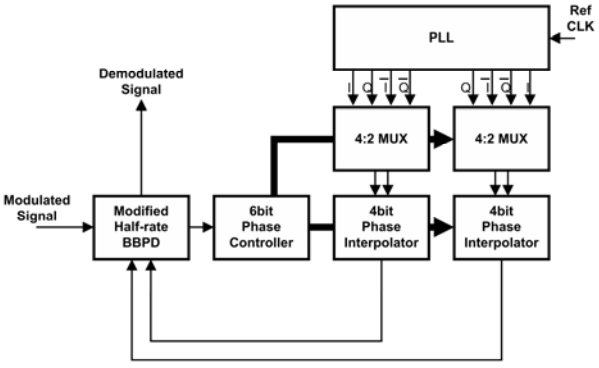

Fig. 8. Block diagram of the proto-type chip

III. Implementation

Fig. 7 shows the structure of half-rate bang-bang PD used in our approach. This is essentially the same as the PD given in [6] except two MUXs having one inverted input are added for implementing the desired inverting function. Although only one MUX is needed, another one is added as a dummy block to match delay. This PD produces two states, lead or lag. For CDR applications, there can be a problem in that wrong output is produced when there is no transition. But in BPSK applications, this is not a problem because BPSK signal always goes through transitions.

The proto-type chip was designed using the phase control algorithm given in [7]. The phase controller has 6bit phase resolution in this design. The proto-type chip has two phase interpolators using the same 6-bit resolution phase controller and different phases from PLL as shown in Fig. 8, because the half-rate bang-bang PD needs multi-phase clocks [8]. The proto-type chip was fabricated using TSMC 0.18 μm CMOS technology.

IV. Measurement

Table I shows the performance of the fabricated chip. The maximum error-free data rate achieved in the back-to-back link was 622Mb/s, which is about half of carrier frequency (1.4GHz). Fig. 9 shows 622Mb/s input data (upper) and demodulated data (lower).

We also measured the link performance with CATV lines with the setup shown in Fig. 10. An LPF limits bandwidth of the transmitting data. Impedance matching circuits are added at both ends of CATV line, since CATV lines have impedance of 75 ohm. Although the measurement doesn't include CATV signals, a HPF is used at the end of CATV line, which can filter out CATV signals. A limiting amp is also added.

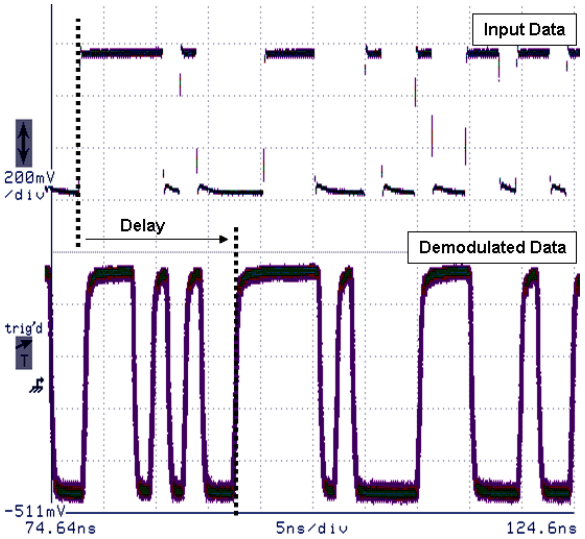

Fig. 9. Demodulation for 622Mb/s data (back-to-back link)

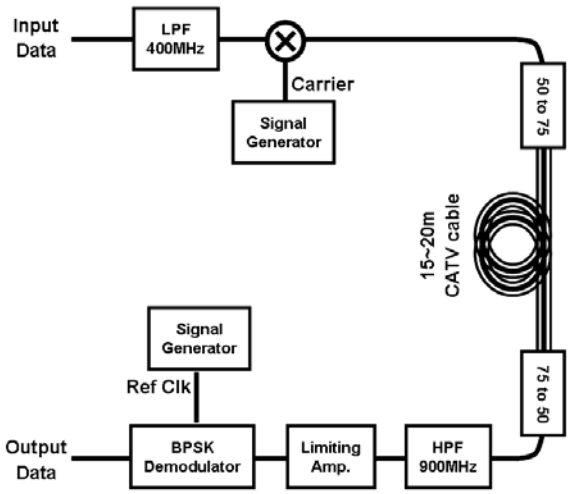

Fig. 10. Fig. 10. Measurement setup

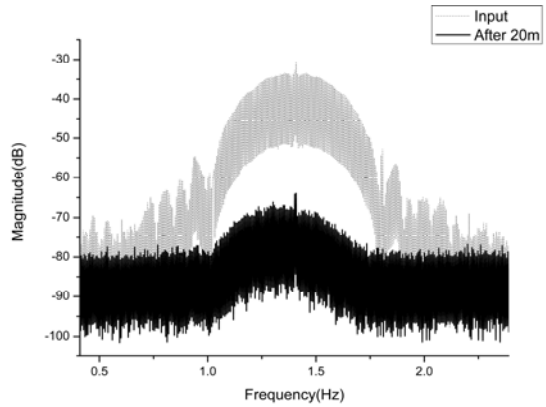

Fig. 11. Fig. 11. Loss in 20m CATV line

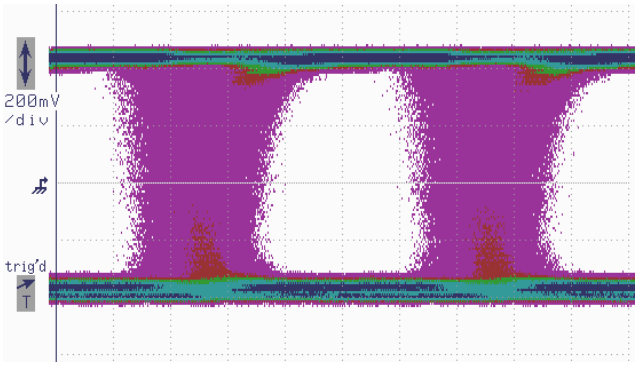

Fig. 12. Fig. 12. Eye diagram of demodulated data (after 20m CATV line)

Fig. 11 shows the spectrum of 400Mb/s BPSK data, which satisfies the IEEE 1394 half-duplex mode [9], at 1.4GHz carrier. The dotted line is the spectrum of the mixer output and the solid line is of signals after 20m CATV line transmission. As can be seen, the peak power decreased by 35dB through 20m cable transmission. In addition, the spectrum becomes asymmetric since high-frequency signals suffer more loss. Fig. 12 is the eye-diagram of data demodulated by the fabricated chip after 20 m transmission. Clear eye opening can be observed. Measured BER was 5×10^{-11} for 15m, 5×10^{-10} for 20m CATV line, and no error was detected for shorter cables.

TABLE I.
PERFORMANCE OF FABRICATED CHIP

Process	TSMC 0.18 ㎛
Maximum data rate (PRBS 2^7-1)	622 Mb/s
Carrier frequency	1.4GHz
Demodulator core area	210 × 150 ㎛ ^{2}
Supply voltage	1.8 V
Power consumption	288mW (including I/O & PLL)

V. CONCLUSION

We demonstrated a new mixed-mode demodulating scheme which can handle a very high data rate compared with the carrier frequency. The demodulator was realized with 0.18 ㎛ CMOS technology. Experimental results show that the proposed scheme can be used for the demodulation of BPSK signals up to 622Mb/s, about half of the carrier frequency.

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[9] IEEE Standard for a High Performance Serial Bus, IEEE Standard 1394-1995.