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09:00~10:30 좌장 : 박재형(충북대)



## 학술발표 T1C 광통신(I)

09:00~10:30 좌장 : 이상수(ETRI)



## 학술발표 T1D 광섬유센서

09:00~10:30 좌장 : 송민호(전북대)

# A 4×10-Gb/s Optical Receiver and VCSEL Driver Array in 0.13-μm CMOS Technology

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Abstract

A 4-channel 10-Gb/s optical receiver and VCSEL driver array are implemented in 0.13-um CMOS technology. To enhance the bandwidth of the optical receiver, a limiting amplifier using a negative impedance compensation and active feedback is proposed. A single channel receiver achieves 96-dBΩ trans-impedance gain ($Z_T$), 10-Gb/s operations with 7.1-GHz bandwidth for 0.25-pF input parasitic capacitance and 23-pA/sqrt(Hz) input noise spectral density that corresponds to -18-dBm sensitivity for $10^{-12}$ BER. The optical transmitter drives VCSEL array, operating up to 10-Gb/s with APC (5-15mA) and AMC (5-20$mA_{PP}$) loops to obtain constant and reliable optical power outputs.

## I. Optical Transceiver Array

An optical link, as shown in Fig. 1, primarily consists of an optical transmitter, which encodes electrical data to optical signals, an optic channel such as plastic optical fiber, which carries optical signal to its destination, and an optical receiver, which reproduces the electrical data from the received optical signals [1].

In this paper, design and implementation of 4 × 10-Gb/s optical receiver and transmitter arrays are reported. Each transmitter incorporates a LVDS/ CML (low voltage differential signal / common mode logic) input buffer, a preamplifier with capacitive degeneration, and a main driver. The pre-amplifier boosts high frequency gain by using the Cherry-Hooper topology. Then, it is followed by an output stage designed to drive large currents (max. 20$mA_{PP}$) at 10-Gb/s. Therefore, the main transistor should be wide enough to drive large currents. However, it might degrade the 3-dB bandwidth and thus the width should be optimized. $I_{MOD}$ represents the modulation current of output driver, corresponding to the optical output swing range, whereas $I_{BIAS}$ is the bias current which corresponds to the average transmitted optical power.

The receiver array consists of TIA (trans-impedance amplifier) and LA (limiting amplifier). For TIA, a number of tradeoffs exist between bandwidth, photodiode capacitance, trans-impedance gain, and noise performance [2]. To overcome this tradeoff, advanced common-gate input configuration is exploited. Simple common-gate configuration has a low input resistance, ~$1/g_m$. However, due to poor device characteristics of CMOS transistors, simple common-gate stage cannot entirely isolate the photodiode capacitance. Therefore, the advanced common-gate stage adding the local feedback stage is exploited. This input stage provides virtual ground input resistance of $1/(1+g_{mB}R_B)g_{m1}$, where $(1+g_{mB}R_B)$ is the voltage gain of the local feedback stage. The gain stage of TIA is designed to be common-source amplifier with feedback resistance ($R_F$). And the dc-cancellation stage is designed to $f_T$ doubler type for this block to prevent total bandwidth reduction. In conventional LA, the inductive peaking technique based on an active inductor, a LC-ladder filter network, or a series passive inductor, has been used to enhance the bandwidth [3]. However, such problems exist as the large passive inductor area, voltage headroom, and gain fluctuation. To solve these problems, we propose a limiting amplifier using negative impedance compensation (NIC) and an active feedback circuit as shown in Fig. 2. Active feedback between two simple common-source amplifiers can improve GBW of the gain stage. A negative transconductance feedback $G_{mf}$ returns a fraction of the output to the input of $G_{m2}$. Because this architecture doesn't resistively load the trans-impedance stage, the total bandwidth of the amplifier can be enhanced. However, intermediate node (A) between two common-source stages exhibits three active devices (M2, M5, and M7) and load capacitors ($C_{L1}$, $C_{L2}$) of the amplifier. Thus, this node is very capacitive. To compensate this parasitic capacitance, NIC technique is added.

## II. Measuremetnt Results

Fabricated optical receiver and transmitter chipsets are measured using a whole optical links. The

designed transmitter drives 4-channel VCSEL array, operating up to 10-Gb/s with APC (auto-power control) of 5-15mA and AMC (auto-modulation control) of 5-20mApp to obtain constant and reliable optical power outputs. The whole 4-channel transmitter array chip occupies the area of 2.05mm x 0.83mm, Fig. 3(b), and dissipates 200-mW from a single 1.8-V supply. Fig. 4 shows eye diagrams for the receiver in the complete optical link. A single channel optical receiver achieves 10-Gb/s operations, 96-dBΩ trans-impedance gain, and 23-pA/sqrt(Hz) input noise spectral density that corresponds to -18-dBm sensitivity for $10^{-12}$ BER. The whole receiver array chip occupies the area of 1.79mm x 1.35mm, Fig. 3(a), and the power consumption is 54-mW from a single 1.2-V supply.

## REFERENCES


[1] W. S. Oh, and K. Park, "Design of a 12-channel 120-Gb/s optical receiver array in 0.18-um CMOS technology," *IEEE Proc. of DELTA*, pp. 71-74, Jan 2008.

[2] Zhenghao Lu, et al., "Broad-band design techniques for transimpedance amplifiers", *IEEE Transactions on Circuits and Systems*, vol. 54, pp. 590-600, 2007.

[3] Wei-zen Chen, and Chao-Hsin Lu, "Design and analysis of a 2.5-Gbps optical receiver analog front-end in a 0.35-um digital CMOS technology," *IEEE Transactions on Circuits and Systems*, vol. 53, pp. 977-983, 2006.


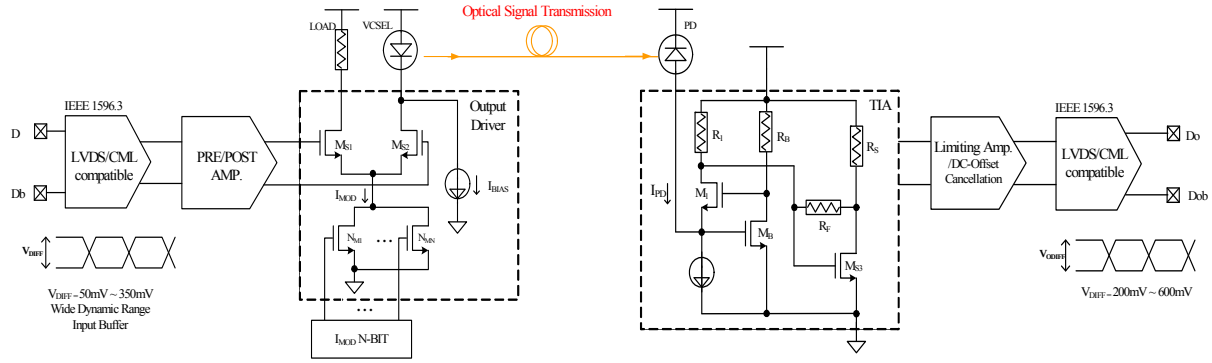


Fig. 1. Implemented optical links using a fabricated optical receiver and transmitter chipsets.

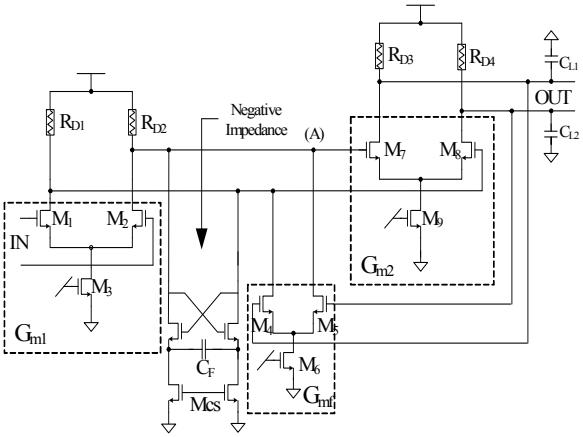


Fig. 2. Proposed limiting amplifier using a negative impedance compensation and active feedback circuit

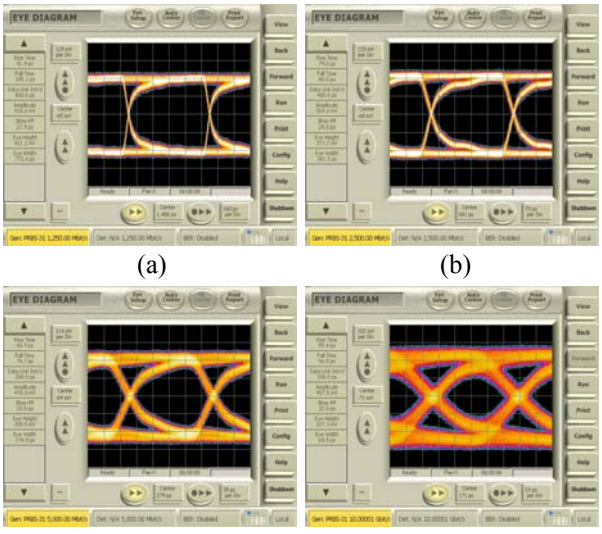


Fig. 4. Eye diagrams at data-rate of
(a) 1.25-Gb/s, (b) 2.5-Gb/s, (c) 5.0-Gb/s, and (d) 10-Gb/s

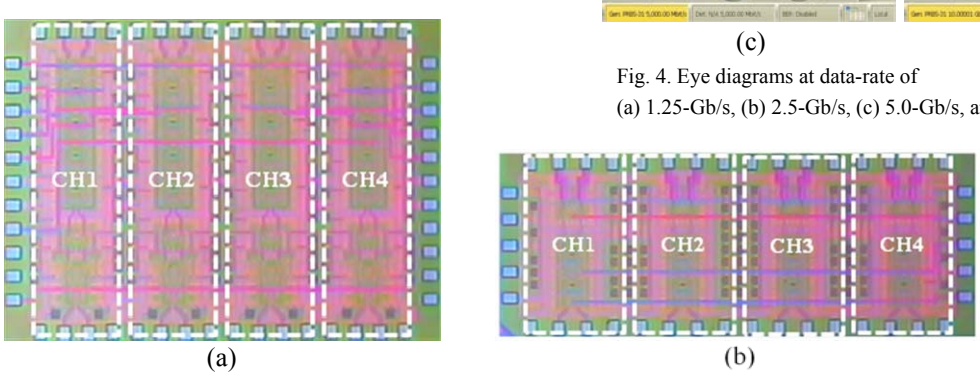


Fig. 3. Micro-photographs of (a) 4-channel optical receiver, and (b) 4-channel VCSEL driver