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A CMOS-Compatible Schottky-Barrier Diode Detector for 60-GHz Amplitude-Shift Keying (ASK) Systems

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***Abstract* — A square-law detector for 60-GHz amplitude-shift keying (ASK) systems is implemented by using CMOS-compatible Schottky-barrier diodes (SBDs). The SBDs fabricated in the 0.18-µm CMOS technology have the cut-off frequency of 250 GHz. The fabricated detector has minimum conversion loss of 23.7 dB at the input carrier and RF power of -3 dBm, and has 3-dB bandwidth of 3 GHz. Using the fabricated detector, 622-Mb/s data transmission in the 60-GHz ASK system is demonstrated with 60-GHz variable attenuators instead of antennas. The bit error rate of 10^{-10} is achieved at the calculated propagation distance of 1.3 meter, and 10^{-6} at 2.5 meters, assuming the Tx and Rx antenna gain of 24 dBi.**

***Index Terms* — amplitude-shift keying, CMOS, Schottky-barrier diode, square-law detector, wireless personal area network**

I. INTRODUCTION

Recently, communications using the 60-GHz band have been enthusiastically studied. The 60-GHz band provides unlicensed band of 7-GHz bandwidth for several Gb/s data transmission. Furthermore, short-range transmission due to high atmospheric absorption and high-directional signal propagation with small-size and high-gain antennas is possible [1]. Standardization of 60-GHz band wireless personal area network (WPAN) has been pursued in the IEEE 802.15 TG3c [2]. For the realization of conventional 60-GHz WPAN systems based on single-carrier or OFDM-based schemes, low-cost development of high-performance RF transceivers and high-speed mixed-mode circuits are required. However, conventional systems have challenges in terms of high linear power amplifiers, low phase noise frequency synthesizers [3], and high-speed analog-to-digital converters for high-rate sampling of several Gb/s data. These burdens lead higher cost for the use of high-performance semiconductor processes and slower time to market than market growth.

In order to overcome these problems, the amplitude-shift keying (ASK) communication scheme can be an alternative solution. Even though ASK modulation has poor spectral efficiency of below 1 bit/Hz, ASK systems offer several advantages [4]. In ASK systems, the modulated signal can be demodulated by square-law devices such as Schottky-barrier diode detectors without any frequency synthesizers and clock recovery circuits at the receiver. In addition, performance requirements of frequency synthesizers at the transmitter are relaxed because problems caused by phase noise and frequency offset are eliminated at the receiver [5]. Moreover, the ASK-modulated signal has relatively low peak-to-average power ratio (PAPR). Consequently, the linearity problem of power amplifiers is mitigated. Besides, analog-to-digital conversion overhead is substantially reduced because digital data are directly modulated to and demodulated from the RF band. Therefore, 60-GHz ASK systems can be an interesting solution for broadband communications especially between portable devices requiring low-cost, low-complexity, and low-power transceivers.

The 60-GHz ASK transceiver using Schottky-barrier diode (SBD) detectors in commercial MMICs has been already reported and 3.5-Gb/s data transmission with the 3-meter wireless channel has been demonstrated [6]. However, ASK transceivers in CMOS technologies are more attractive because CMOS technologies enable single-chip integration of RF circuits and digital circuits in a cost-effective manner. It is previously reported that SBDs having cut-off frequencies of 400 GHz ~ 1 THz can be fabricated in CMOS technologies [7]-[8], and detectors using SBDs are applicable [9]-[10].

In this work, we fabricate Schottky-barrier diodes in the standard 0.18-µm CMOS technology. Using them, we implement the 60-GHz square-law detector for ASK receivers and demonstrate 622-Mb/s data transmission in the 60-GHz ASK system.

II. SCHOTTKY-BARRIER DIODES IN CMOS TECHNOLOGY

The SBD for 60-GHz square-law detectors was fabricated in the standard 0.18-µm CMOS technology. Schottky contacts of the SBD are formed between the cobalt salicide layer and the low-doped n-well layer without n+ source/drain implantation. To achieve the cut-off frequency of SBDs much higher than 60 GHz, 25 SBD cells are configured in parallel. The Schottky contact area of each cell is minimized into 0.46 x 0.46 µm^2 allowed by the process [8].

To evaluate the cut-off frequency of the fabricated SBD, 1-port S-parameter of the SBD was measured in the on-wafer measurement setup. The diode resistance and capacitance extracted from S-parameter are about 20 and 32 fF. The calculated cut-off frequency is approximately 250 GHz. Compared with the previously reported SBD having the cut-off frequency of 400 GHz [7], the fabricated device has the relatively low cut-off frequency. The lower cut-off frequency

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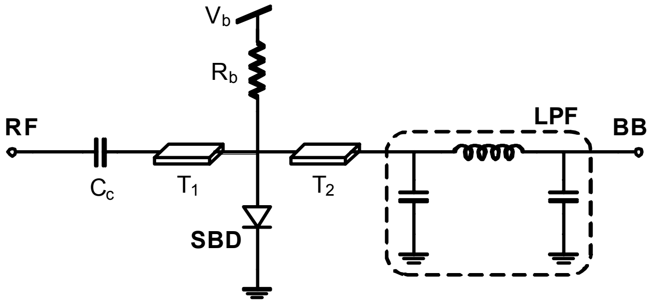

Fig. 1. Schematic of 60-GHz square-law detector

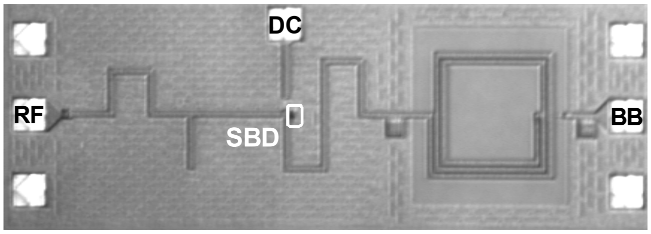

Fig. 2. Chip-photo of fabricated 60-GHz square-law detector

characteristics are possibly due to the higher resistive n-well region of the CMOS technology used in this work.

III. 60-GHz SQUARE-LAW DETECTOR

A. Circuit Description

Fig. 1 and Fig. 2 show the schematic and the chip photo of the 60-GHz square-law detector based on single shunt diode configuration using the 25-cell SBD. The bias voltage of the SBD is optimized to obtain maximum conversion efficiency. The bias circuit is simply configured using the 2-k N+ poly resistor R_b and the 1-V bias voltage V_b. For isolation between the RF input port and the baseband output port, the 100-fF coupling capacitor C_c and the low-pass filter (LPF) are used. The LPF is designed to have the cut-off frequency of 4.5 GHz and high rejection of 60-GHz signals. For the LPF, 800-fF capacitors and a 3-nH inductor are chosen. The transmission line T_1 and T_2 as matching networks are implemented using microstrip lines. T_1 is the input conjugate matching network including 50- transmission lines and an open stub. T_2 is the quarter-wavelength line at 60 GHz to transform low input impedance of the LPF to high impedance at 60 GHz [11]. Additionally, an external DC blocker is added at the output port. All capacitors and inductors in the circuit are fabricated using metal-insulator-metal (MIM) capacitors and spiral inductors. Microstrip lines are realized using the top-metal layer for signal lines and the bottom-metal layer for a ground plane. DC power consumption of the detector is 325 μW.

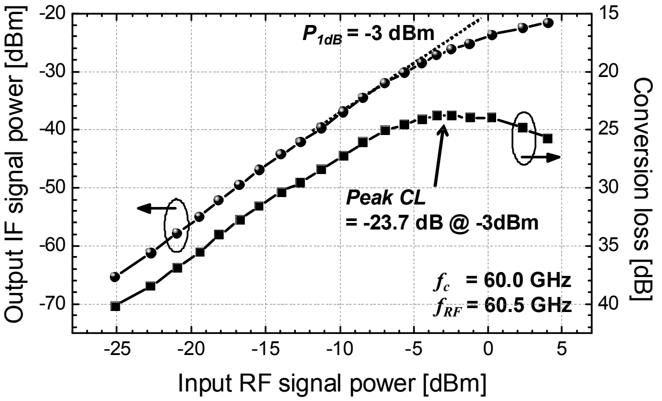

Fig. 3. Output IF output power and conversion loss of detector versus input RF signal power

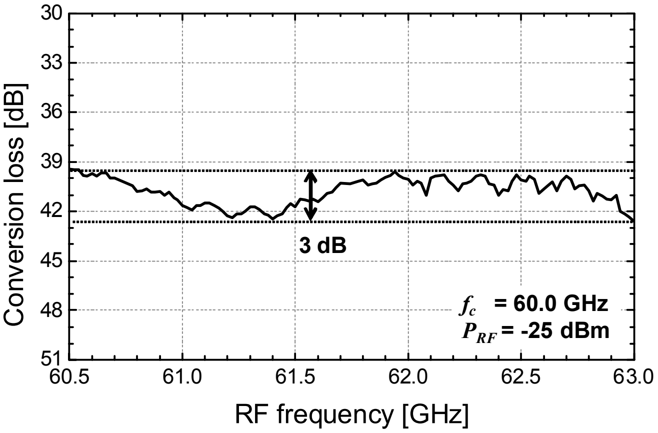

Fig. 4. Conversion loss of detector versus RF frequency

B. Experimental Results

The fabricated 60-GHz square-law detector was measured in the on-wafer setup. Power loss from RF probes and cables and non-flat frequency response of generated input signals were deembedded to investigate the intrinsic performance of the detector. Fig. 3 shows the output IF signal power and the conversion loss versus input RF signal power at the RF and carrier frequency of 60.5 GHz and 60 GHz, respectively. The carrier signal power was set to the same as the input RF signal power. The measured output IF signal power increases with the slope of 2 due to the square-law operation in the low input power region. In the high input power region, the output IF power is compressed because the large voltage swing at the diode decreases the conversion efficiency. The input 1-dB compression point is about -3 dBm. The conversion loss of the detector decreases with the slope of 1. The minimum conversion loss of about 23.7 dB is obtained at the input power of -3 dBm. The fabricated detector has the relatively high conversion loss because of no large LO pumping and high series resistance of the diode. If the number of SBD cells

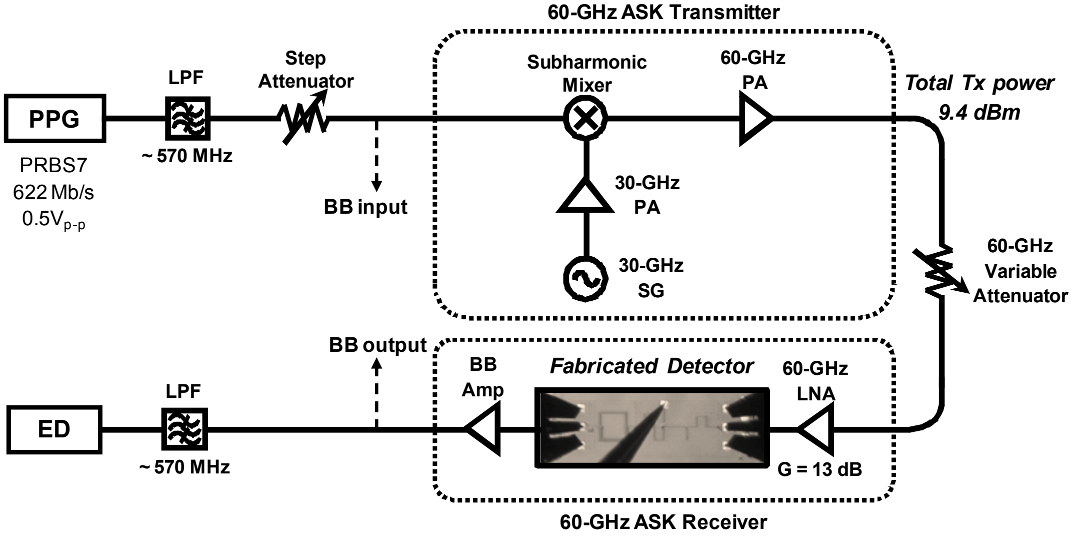

Fig. 5. Experimental setup for 60-GHz ASK system

is increased in parallel, the series resistance is lower. Therefore, the conversion loss can be reduced.

Fig. 4 shows the conversion loss as a function of RF frequency when the input RF power is -25 dBm. In the frequency range of 60.5 ~ 63.0 GHz, the variation of the conversion loss is within 3 dB at the fixed carrier frequency of 60 GHz. In our experimental setup, the conversion loss measurement was impossible in the frequencies of below 60.5 GHz. From the results, the detector can cover baseband frequencies of 100 kHz to 3 GHz with the DC blocker, which has cut-off frequency of 100 kHz.

IV. BROADBAND DATA TRANSMISSION IN 60-GHZ ASK SYSTEM

To investigate the feasibility of the fabricated 60-GHz square-law detector for 60-GHz ASK systems, broadband data transmission in the 60-GHz ASK system was demonstrated with 622-Mb/s baseband data. Fig. 5 shows the experimental setup for the 60-GHz ASK system. The input data, 622-Mb/s NRZ 2^7-1 word length pseudorandom binary sequence, are generated by a pulse pattern generator. After filtering out the outside band of data with a LPF, baseband data are directly modulated to the 60-GHz ASK signal using a simple frequency up-conversion technique with a subharmonic mixer.

The modulated ASK signal consists of both the up-converted baseband signal and the 60.0-GHz LO leakage signal. The powers of these two signals are tuned to have same level by controlling the step attenuator. The total transmitter output signal power at the power amplifier output is set to 9.4 dBm. Instead of antennas, 60-GHz variable attenuators between the transmitter and the receiver are used for accounting for path loss between antennas without considering multi-path fading effects. The RF receiver is simply configured with the LNA having a gain of 13 dB, the fabricated detector, and a baseband amplifier, without local oscillators. The performance of transmission is examined using a spectrum analyzer and an error detector. Fig. 6 shows

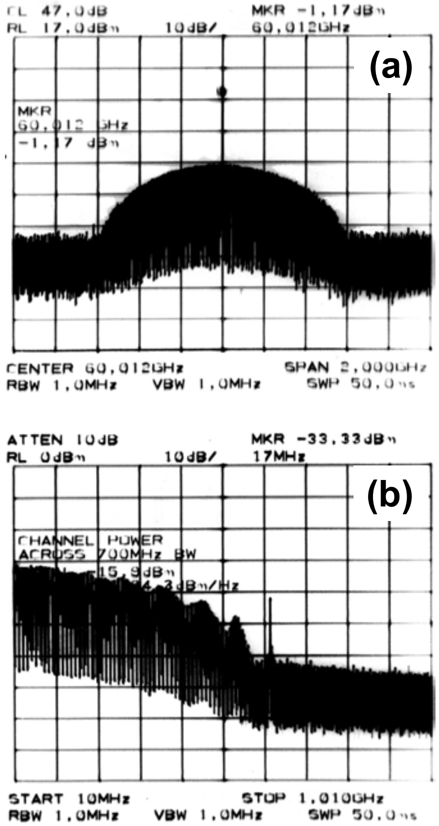

Fig. 6. Spectra of (a) Transmitter output signal and (b) detected baseband signal

the spectra of the transmitter output signal and the detected baseband signal when the received signal power at the input of 60-GHz receiver is -13 dBm.

Fig. 7 shows the bit error rate (BER) performance as functions of the total RF received signal power and the corresponding estimated propagation distance. The total RF received signal power was swept by changing the attenuation level of 60-GHz attenuators. The propagation distance is calculated from the attenuation level, assuming that wireless transmission uses 24-dBi Tx and Rx directional antennas. The BER performance achieves below 10^{-10} at the RF received signal power higher than -13 dBm, or at the calculated propagation distance of about 1.3 meter. The inset in Fig. 7 shows the eye diagram of the detected baseband signal at the received signal power of -13 dBm. At the BER of 10^{-6} which is an acceptable value in wireless communications, the calculated propagation distance is about 2.5 meter. For considering file-transfer applications between portable devices, one of the mandatory 60-GHz WPAN usage models, the distance coverage of 1 meter is required [12]. Experimental results show that 60-GHz ASK systems using CMOS SBD detectors satisfy the usage model at the data rate of 622 Mb/s.

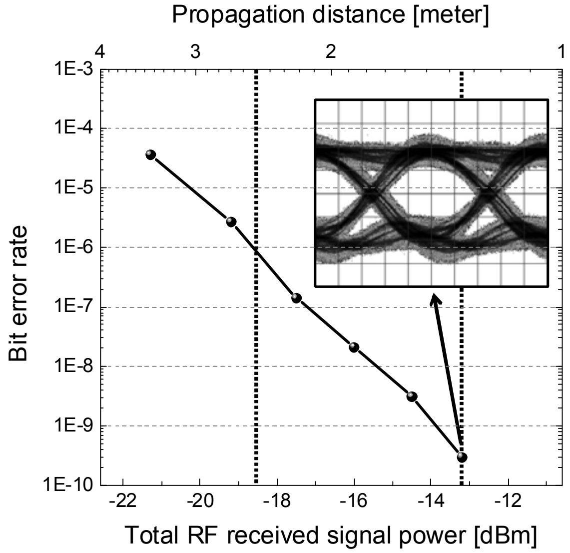

Fig. 7. Bit error rate versus total RF received signal power and calculated propagation distance (Tx/Rx antenna gain of 24 dBi each)

V. CONCLUSION

The 60-GHz square-law detector utilizing Schottky-barrier diodes in the standard 0.18-μm CMOS technology is developed and evaluated. 622-Mb/s broadband data transmission in the 60-GHz ASK systems is demonstrated with the BER of 10^{-6} at the calculated propagation distance of 2.5 meters. Experimental results guarantee the usability of CMOS-based low-cost and low-complexity 60-GHz ASK systems. Gigabit data transmission will be possible if the performance of the detector is enhanced by further improvement in detector design techniques.

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