

제17회 한국반도체학술대회

The 17th Korean Conference on Semiconductors
“Semiconductor for Human and Eco”

초대의 말씀

조 직

목 차

- 일시 2010년 2월 24일(수) ~ 26일(금)
- 장소 호텔 인터불고 엑스코(유통단지 내), 대구



- 2010년 2월 25일(목)
Plenary Session
구두발표
포스터 발표
Chip Design Contest

- 2010년 2월 26일(금)
구두발표
포스터 발표

검 색

나 가 기



주관 경북대학교 - 반도체융합기술연구원, 센서기술연구소, 반도체공정교육 및 지원센터, 디스플레이 기술교육센터, 기능성소자융합플랫폼연구센터, World Class University 포항나노기술집적센터, 영남대학교 LED-IT 융합산업화연구센터, 한국반도체산업협회, 한국반도체연구조합

주최 한국물리학회 반도체분과회, 한국재료학회, 대한전기학회 전기재료연구회, 대한전기학회 MEMS 연구회, 대한전자공학회 반도체재료 및 부품연구회, 대한전자공학회 SoC 설계연구회, 반도체설계교육센터(IDEC)

후원 대구광역시, 대구컨벤션뷰로, 삼성전자, 하이닉스반도체, 한국전자통신연구원, 동부하이텍, (주)실리콘웍스, (주)피케이엘, (주)에스엔에스텍, (주)티에스이, (주)아론, (주)시스넥스, (주)울텍, (주)아이엔씨테크놀로지, (주)케이시텍, (주)루멘스, IEEE Electron Device Society Korea Chapter, IEEE SSC Seoul Chapter



2010년 2월 25일(목) 15:00-16:20

TF3

Room A 블루벨홀	Room B 아이리스홀	Room C B101	Room D B102	Room E B103	Room F B108	EXCO 지하 1F Lobby
----------------	-----------------	----------------	----------------	----------------	------------------------	---------------------

세션명 Advanced Analog Techniques
좌 장 이종욱(경희대학교), 류승탁(KAIST)

TF3-1 15:00-15:20

1.62 Gb/s and 2.7 Gb/s Adaptive Equalizer for DisplayPort 1.1a Standard

J. S. Rhim, C. K. Seong, W. S. Kim, and W.Y. Choi
School of Electrical and Electronical Engineering, Yonsei University

An adaptive equalizer is implemented for display port 1.1a standard with 0.13 μm CMOS technology. Overall frequency response of the channel is flattened using high pass filter with current combiner. The adaptation block controls the amount of compensation by comparing the portion between high-frequency and low-frequency components. The fabricated chip consumes 11mW of power from 1.2V supply voltage. The operation of the designed equalizer was verified at both 1.62 Gb/s and 2.7Gb/s for 15m display port cable.

TF3-2 15:20-15:40

An 8-channel 8-Gb/s Optical Receiver Analog Front-End in a 0.13- μm CMOS Technology

박규상¹, 황문상¹, 유병주¹, 김현창¹, 정덕균¹, 박정우², 김경옥²
¹서울대학교 반도체 공동 연구소 집적 시스템 설계 연구실, ²한국전자통신연구원

In this paper, a gain-booster cascode feedback transimpedance amplifier(TIA) is proposed to increase the bandwidth of the optical receiver and relax the design tradeoffs between the bandwidth and the gain. The TIA achieves 57.6-dB Ω transimpedance gain with 6.92-GHz bandwidth for 1-pF input parasitic capacitance. A limiting amplifier(LA) with a DC offset control circuit is also developed to cancel the voltage offset between the positive and negative inputs of the differential signals. By exploiting the TIA and the LA, an 8-channel 8-Gb/s optical receiver analog frontend is designed in a 0.13- μm CMOS process. The simulated 1-channel power consumption without the buffer and the driver is about 56.4 mW for 100- μA peak-to-peak 8-Gb/s 2³¹-1 PRBS input. The 8- channel layout occupies the area of 3.5 x 0.4 mm².

2010년 2월 25일(목)

Abstract

1.62 Gb/s and 2.7 Gb/s Adaptive Equalizer for DisplayPort 1.1a Standard

J. S. Rhim, C. K. Seong, W. S. Kim and W.Y. Choi

School of Electrical and Electronical Engineering, Yonsei University
Shinchondong 134, Seodaemun-Gu, Seoul 120-749, Korea

Abstract

An adaptive equalizer is implemented for display port 1.1a standard with 0.13 μ m CMOS technology. Overall frequency response of the channel is flattened using high pass filter with current combiner. The adaptation block controls the amount of compensation by comparing the portion between high-frequency and low-frequency components. The fabricated chip consumes 11mW of power from 1.2V supply voltage. The operation of the designed equalizer was verified at both 1.62 Gb/s and 2.7Gb/s for 15m display port cable.

1. Introduction

As the required data rate for communication system is increasing, the loss due to the channel bandwidth limitation has become more severe. To reduce data distortion and improve the quality of the signal, an equalizer is introduced at the front-end of the receiver. An equalizer basically compensates the high frequency loss of the bandwidth-limited channel and reduces the Inter-Symbol Interference (ISI) components of the data.

DisplayPort 1.1a is a competitive standard for display interface authorized by Video Electronics Standard Association (VESA) in 2008 [1]. The required data rates are 1.62 Gb/s and 2.7 Gb/s and the length of the cable is from 2 to 15m.

In this paper, an adaptive equalizer for display port 1.1a standard has been designed which consists of high pass filter with current combiner [2] and power comparison adaptation method [3]. Section 2 introduces overall structure of the equalizer and the measurements and the conclusions are shown in section 3 and 4.

2. Adaptive Equalizer Design

The basic structure of the equalizer is shown in Fig.1. The architecture consists of equalizer filter and adaptation block. Equalizer filter is implemented with a high-pass filter with current combiner and the power comparison method is adopted for the adaptation block.

A high pass filter with current combiner is designed for equalizer as shown in Fig.2. In contrast to active high-frequency boosting filters, passive high pass filter in Fig.2 (a) degrades the dc level of the signal, which flattens the overall frequency response of the channel with lower power consumption. The current combiner sums up the high-frequency compensated components with the input data in the form of current by accepting additional tail current of the current mode logic type buffer as shown in Fig2.(b).

Adaptation block compares the ratio of the power between high-frequency and low-frequency components from the output of the equalizer filter and generates the control voltage for current combiner to obtain an optimal equalization point. The output of the equalizer filter is separately filtered with low pass filter and high pass filter as shown in Fig.3. The difference between the power of high-frequency and low frequency components is accumulated in the capacitor C_S . Voltage to current (V/I) converter amplifies the difference of the high-frequency and low-frequency power and generates the control voltage by charging and discharging C_L .

3. Measurement and Results

Fig. 5 shows the layout of the designed equalizer core. The equalizer is implemented with Chartered 0.13 μ m CMOS technology. The total area of the equalizer block is 115 x 115 μ m² and the power consumption is 11mW excluding the output buffer. Designed equalizer operates at both 1.62 Gb/s and 2.7 Gb/s for 15m display port cable as shown in Fig.6. Table.1 summarizes overall performance of the designed equalizer.

4. Conclusion

An adaptive equalizer for display port 1.1a is designed and its performance has been verified. The designed equalizer consists of equalizer filter and adaptation block. The equalizer filter compensates high frequency loss with high pass filter and current combiner. The amount of compensation is adaptively decided with the adaptation block with power comparison method. The equalizer operates at both 1.62 Gb/s and 2.7 Gb/s for 15m display port cable.

Acknowledgement

This study was funded by "A Collaborative Project for Excellence in Basic System IC Technology (System IC 2010)". EDA Tool was supported by IC Design Education Center (IDEC), and the chip fabrication was supported by Silicon Works Inc.

References

- [1] Video Electronics Standards Association, "VESA DisplayPort Standard 1.1a", Jan, 11, 2008.
- [2] Matt Park, "A 7Gb/s 9.3mW 2-Tap Current Integrating DFE Receiver", *ISSCC Dig. Tech. Papers*, pp224-245, Feb, 2007.
- [3] Jri Lee, "A 20Gbps Adaptive Equalizer in 0.13 μ m CMOS Technology", *IEEE Journal of Solid State Circuits*, Vol 41, No. 9, Sep, 2006.

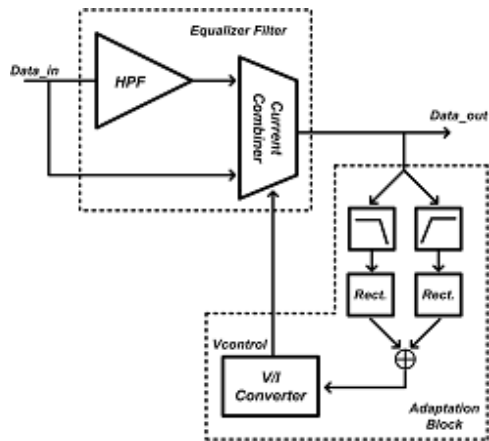


Fig. 1. Block diagram of Adaptive Equalizer

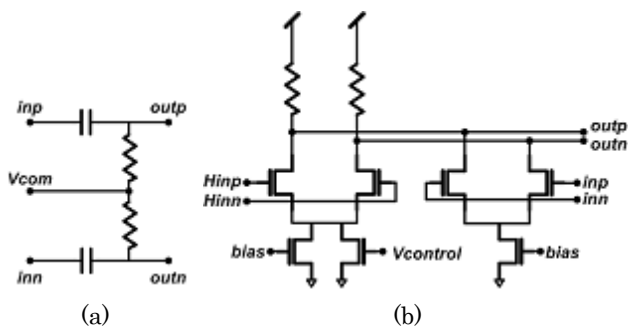


Fig.2. Schematic of High-Pass filter and Current Combiner

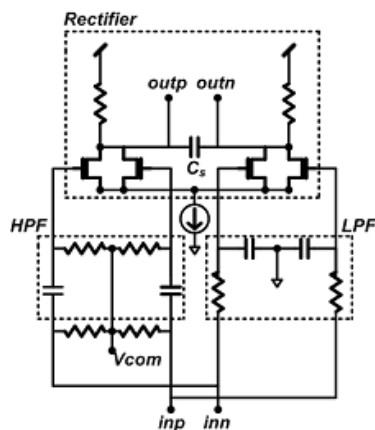


Fig.3. Schematic of Power Detector

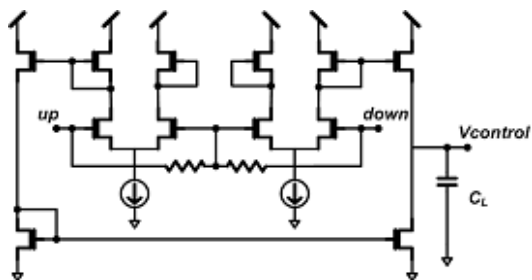


Fig.4. Schematic of V/I Converter

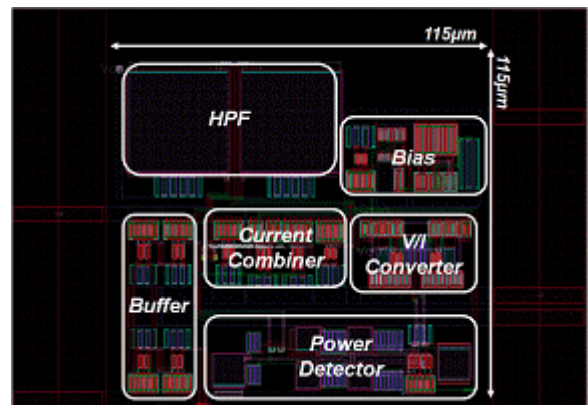


Fig.5. Layout for Equalizer

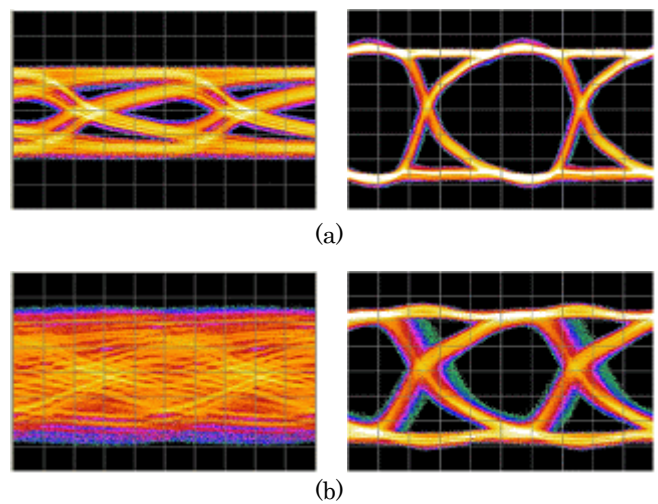


Fig.6. Eye diagram before and after equalization of 15m display port cable at (a) 1.62Gb/p (b) 2.7Gb/s

Table.1. Summary of the Designed Equalizer

Technology	Chartered 0.13µm CMOS Process
Supply Voltage	1.2V
Operation Speed	1.62 Gb/s, 2.7 Gb/s
Channel	15m Display port cable
Power consumption	11mW (excluding output buffer)
Chip Area	115 x 115 µm ²