

Introduction

❖ Topic

- Development of SerDes IP based on 65nm CMOS

❖ Team member

- Team member: K.C Choi, C.K Seong, Y.S Park and W.S Kim
 - CDR (Clock and Data Recovery) part: K.C Choi
 - PLL (Phase-Locked Loops) part: Y.S Park
 - Equalizer part: C.K Seong and W.S Kim

❖ Sponsor

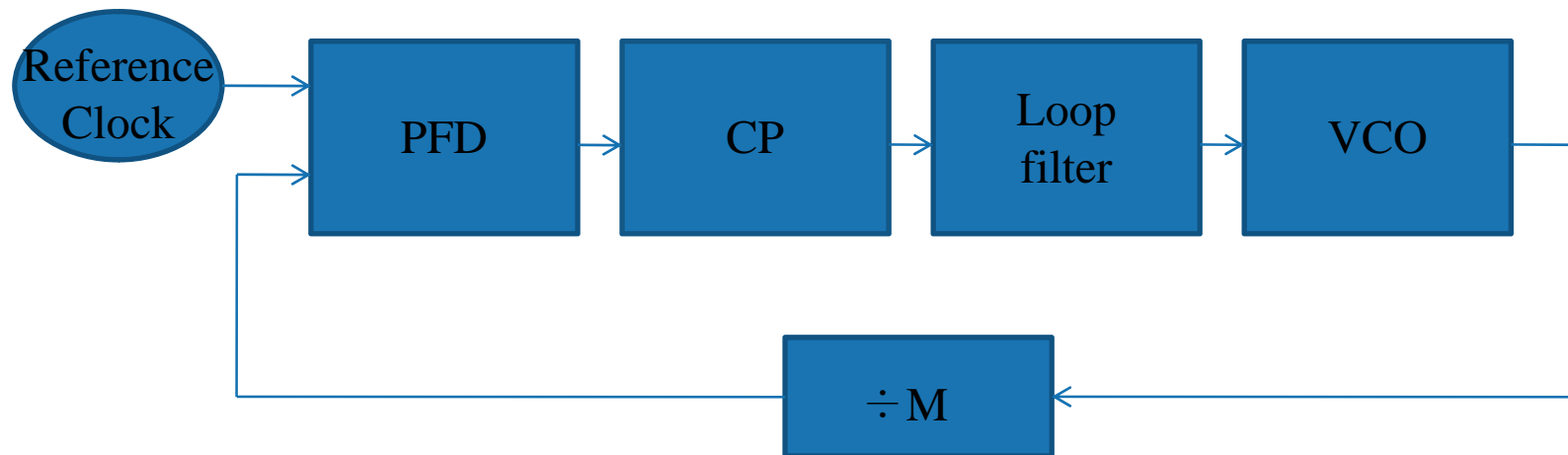
- Samsung Electronics

Phase Locked Loops

❖ Phase Locked Loops

- A PLL serving the task of **clock generation**

❖ Basic Structure



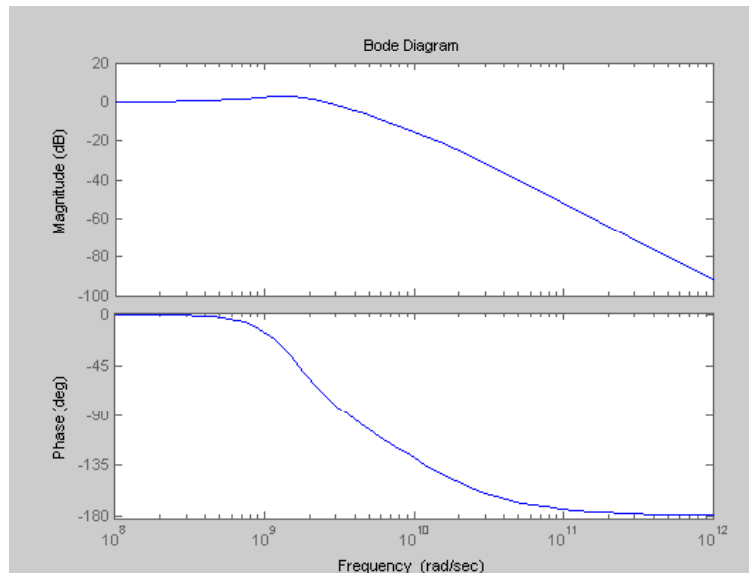
Problems of Phase Locked Loops

❖ PLL jitter

- input reference clock jitter vs. VCO (voltage controlled oscillator) jitter

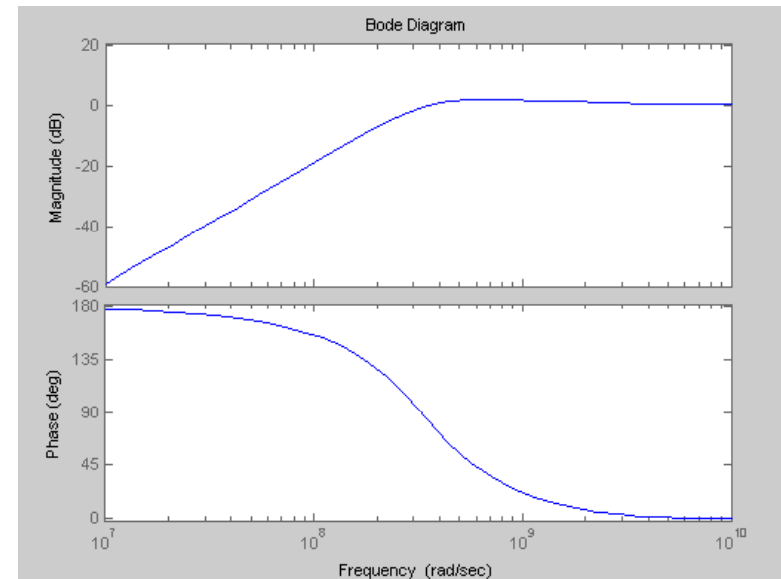
❖ PLL jitter transfer function

- output jitter/reference clock jitter



Low pass filtering

- output jitter/ VCO jitter



High pass filtering



Solutions

❖ Solutions for low jitter PLL

1. Using a low jitter VCO
2. Modifying the structure of a PLL
3. Using the supply voltage regulator to make a supply noise insensitive PLL
4. Find the optimal form of PLL jitter transfer function