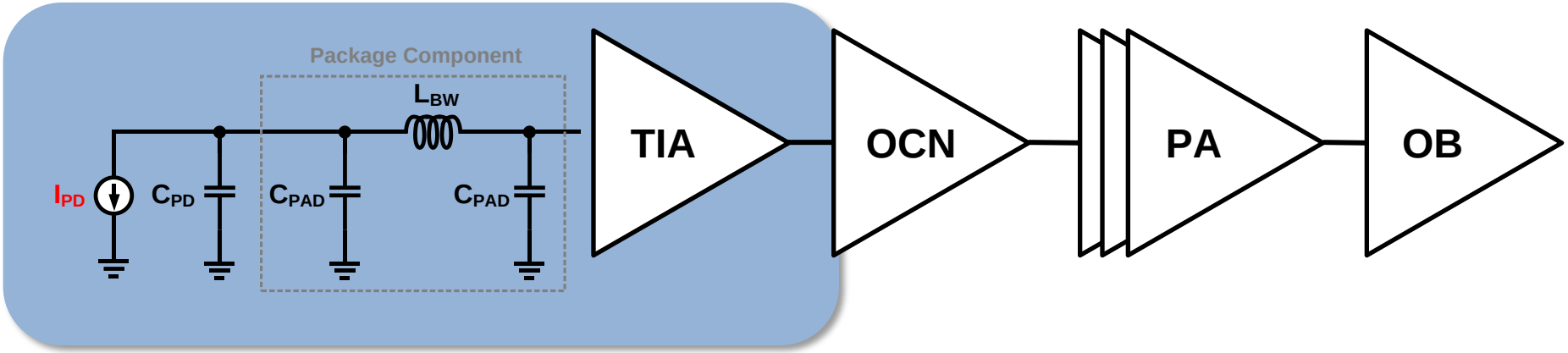
An 20 Gb/s Optical Receiver for Ge-photodetector

- **Optical receiver structure**



I_{PD}: photocurrent source
C_{PD}: photodetector capacitance
C_{PAD}: parasitic PAD capacitance
L_{BW}: bonding wire inductance

- **Designed in *65 nm CMOS* process.**
- **Will be *hybrid-integrated* with *Ge-photodetector* by wire bonding.**
- **Targeted to *20 Gb/s data* transmission.**

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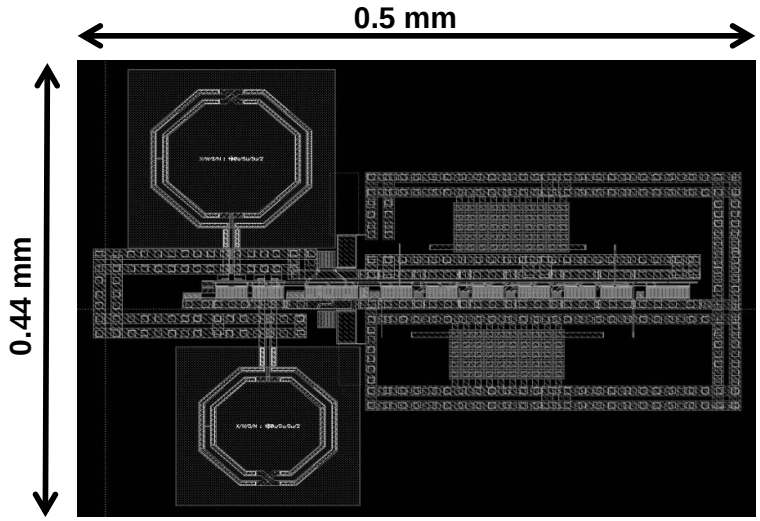
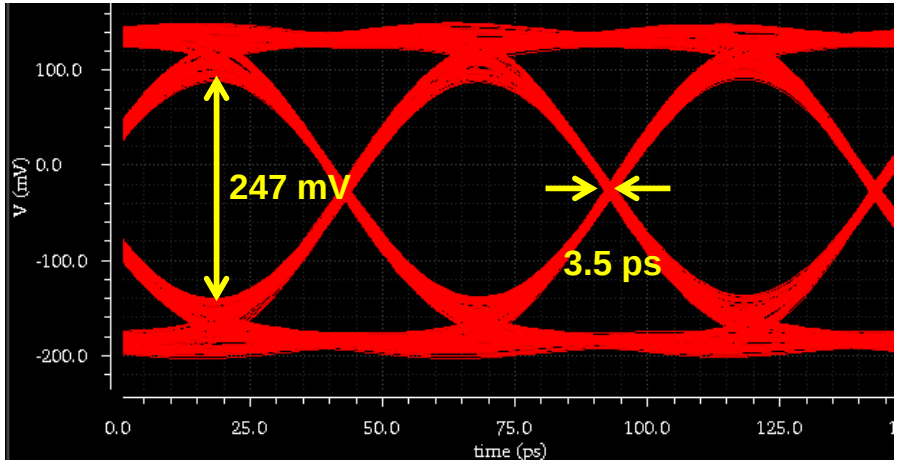
- **MPW 117th SEC 65 nm**



<Chip Layout>



<Post-Layout Simulation (20-Gb/s, 100 uA input)>

	Target	Result (sim.)
Technology	SEC CMOS 65nm	SEC CMOS 65nm
Output V_{p2p}	> 200 $mV_{p-p,diff}$	247 $mV_{p-p,diff}$ (PA)
Bandwidth	14 GHz (TIA), 20GHz (PA)	13 GHz (TIA), 19 GHz (PA)
Chip area	1.5 mm x 1 mm	0.5 mm x 0.44 mm
Power	120 mW (@ 1.2 V supply)	100 mW (@1.2 V supply)