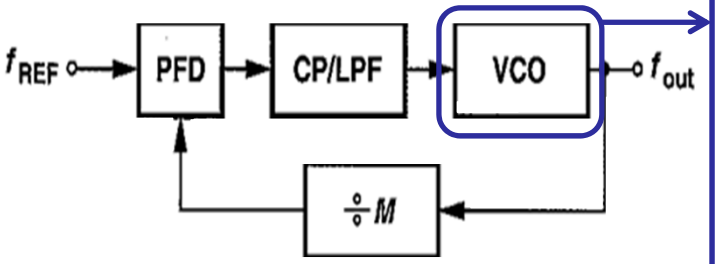
Phase Locked Loop



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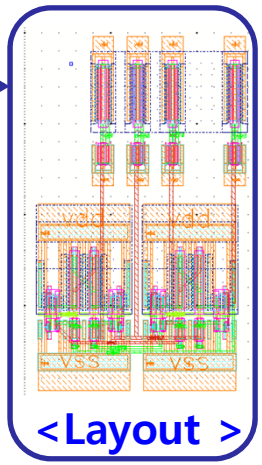
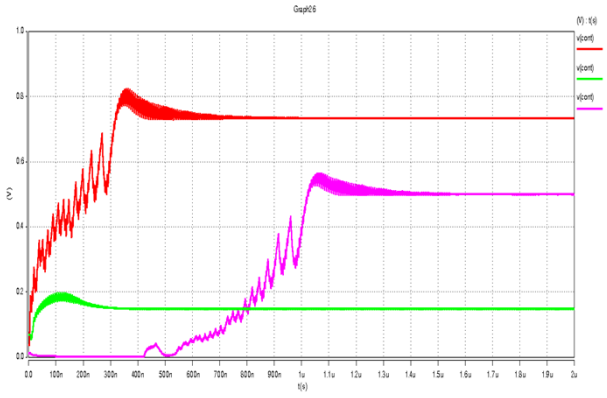


<Layout >

Target Frequency		5 GHz
PLL Blocks		Lee & Kim VCO
		Tri-state PFD
		Replica bias charge pump
		D flipflop based Divider
Power	VCO	2.4mW
	Other blocks	1.9mW
Jitter		0.701 ps(0.0035UI)



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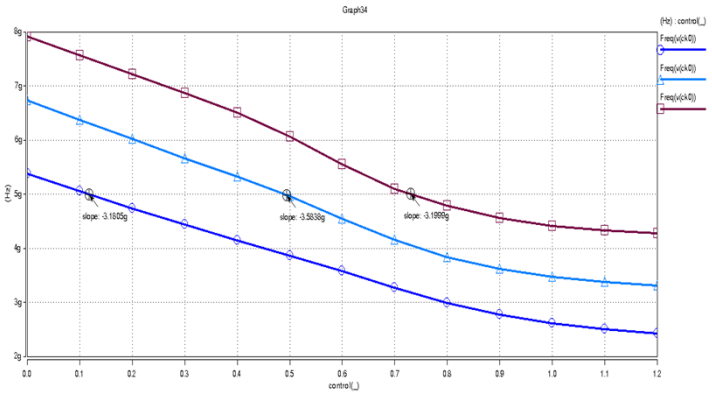

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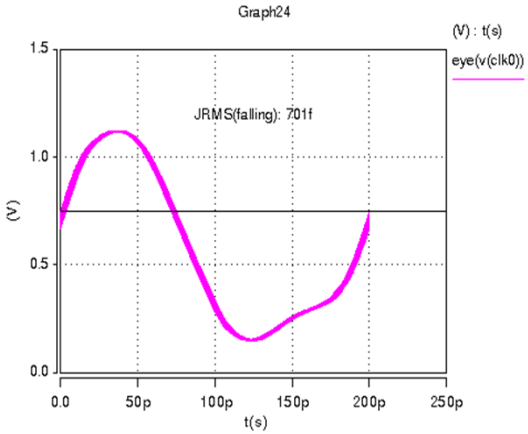
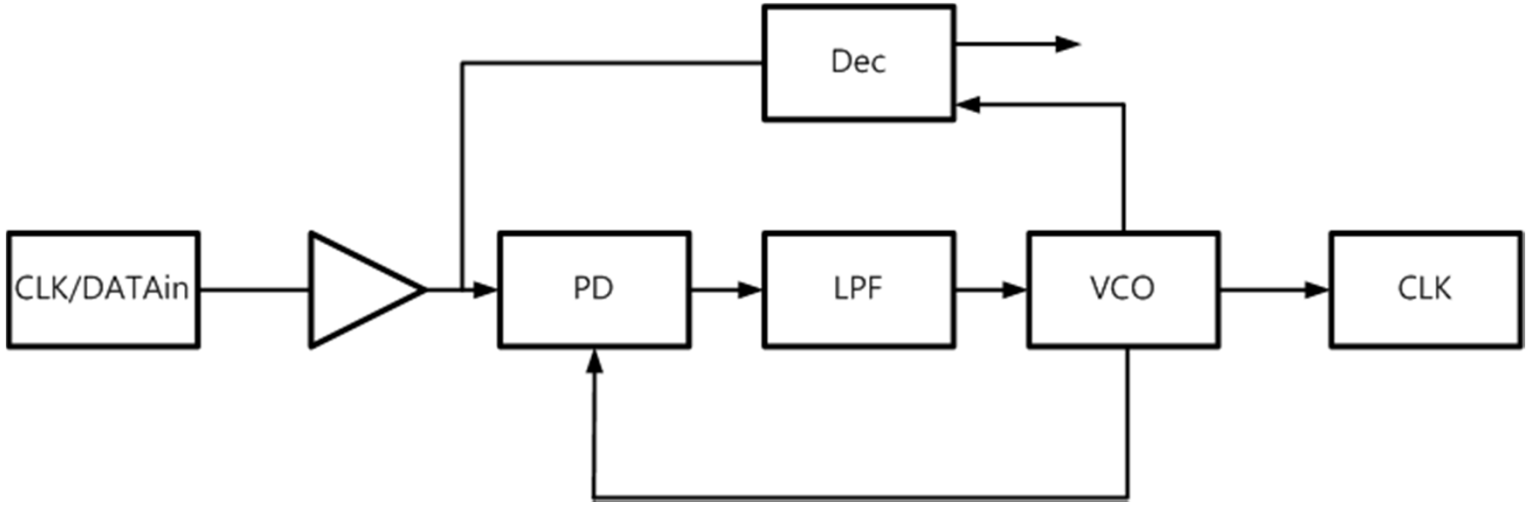


<Eye diagram>

Future Goal

[Clock and Data Recovery]



<Block diagram>

- **CDR is similar to PLL**
- **Future goal is to make 25 Gbps quarter rate CDR**