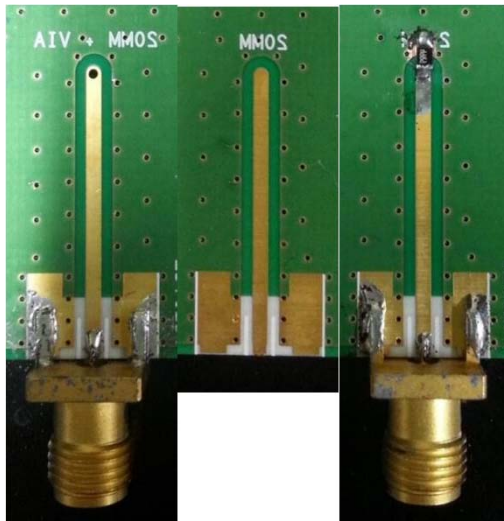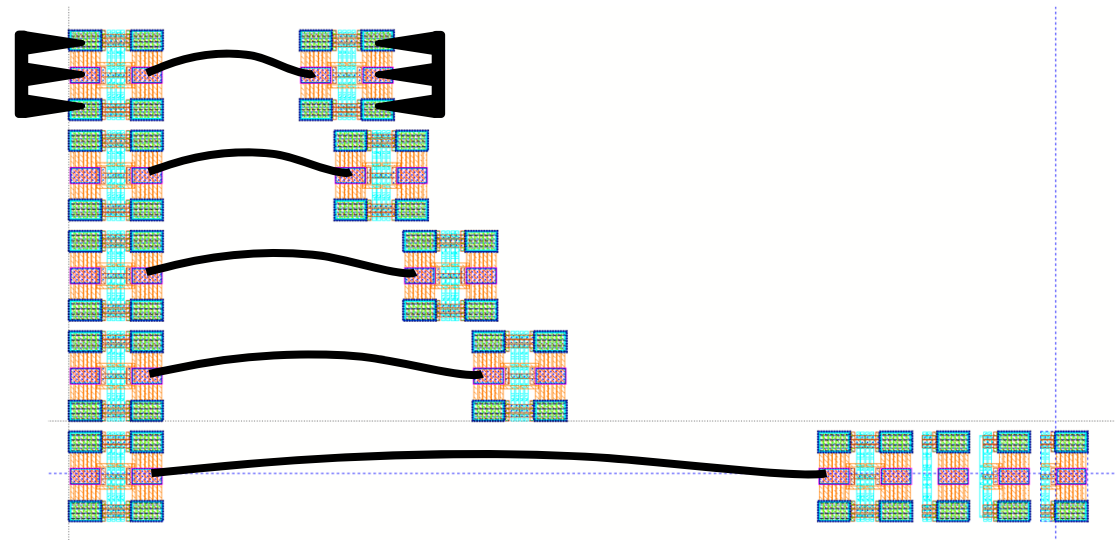# *Bonding wire test*

- For high-speed IC design, bonding wire inductance affects
- **Research goal: <u>Reliable prediction of bonding wire inductance</u>**

**Bonding wire measurement by
SHORT, OPEN, LOAD model
on PCB board**

**Bonding wire measurement by
PAD, OEN, SHORT model on
chip probing**

Low-power TDC

- **Research goal: <u>Design low-power TDC with accurately predictable resolution</u>**
- DLL design: Low-power design, No offset design
- Target application: ADPLL's phase-to-digital converter, considering more…
- Core size: 0.585mm x 0.067mm

	TDC by full-speed DLL	TDC by low-speed DLL
2 * DLLs	**NN: 1.67mW** FF: 1.79mW SS: 1.59mW	**NN: 0.79mW** FF: 0.91mW SS: 0.71mW
Others	**NN: 0.78mW** FF: 0.85mW SS: 0.76mW	**NN: 0.78mW** FF: 0.85mW SS: 0.76mW
Total	**NN: 2.45mW** FF: 2.64mW SS: 2.35mW	**NN: 1.57mW** FF: 1.76mW SS: 1.47mW

MZM bias controller

- **Research goal: <u>Design MZM bias control circuit that can automatically provide optimal bias voltage.</u>**
- Power minimization of pilot tone's 2nd-order harmonic
- IHP's 0.25μm BiCMOS process

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