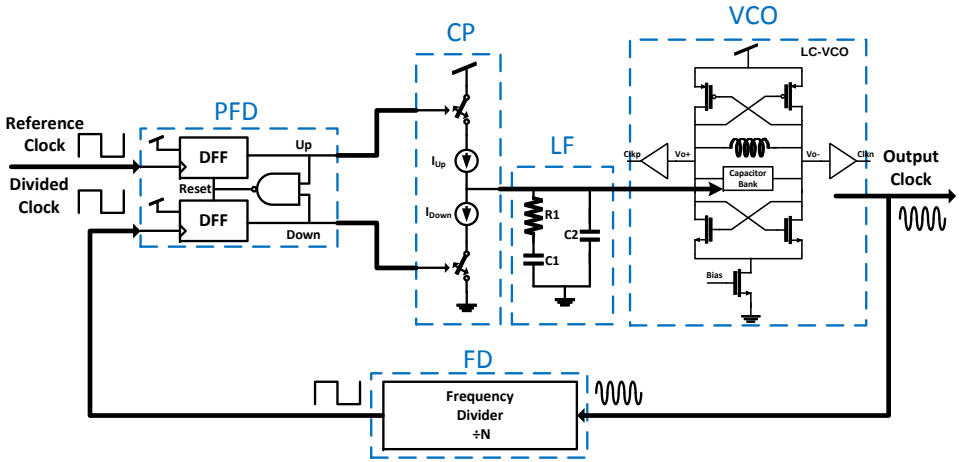
# 12.5-GHz PLL with LC-VCO

- **PLL block diagram**

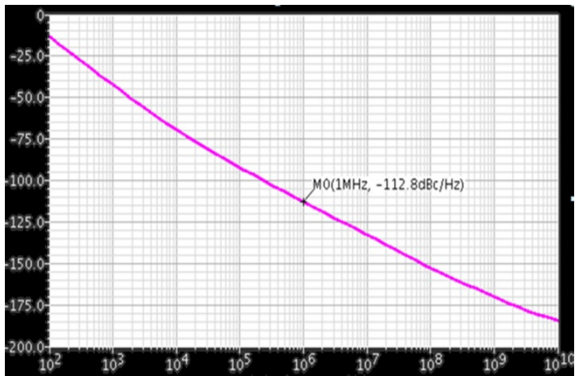



✓ **Simulation results**

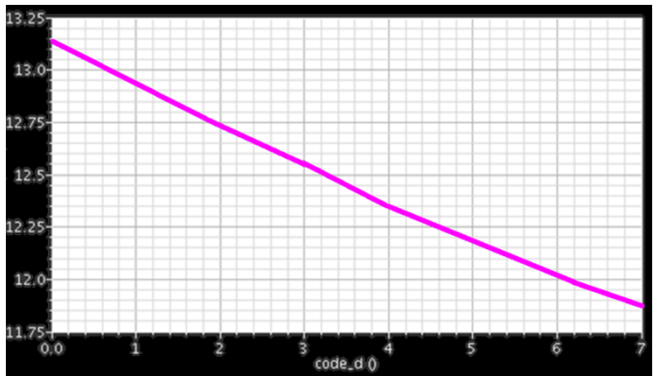
- Frequency tuning range : 11.85 GHz ~ 13.15 GHz
  → Design target : 12.5-GHz
- LC-tank control bit : 3-bit
- VCO Phase noise : -112.8 dBc/Hz @ 1-MHz offset
- VCO Bias current variance : 1-mA ~ 4-mA
  → For stable oscillation start
  → Output swing control
- VCO FOM : -191.3 dBc/Hz

$$FOM = L\{\Delta f\} - 20\log_{10}\left(\frac{f_o}{\Delta f}\right) + 10\log_{10}\left(\frac{P_{DC,core}}{1\text{mW}}\right)$$

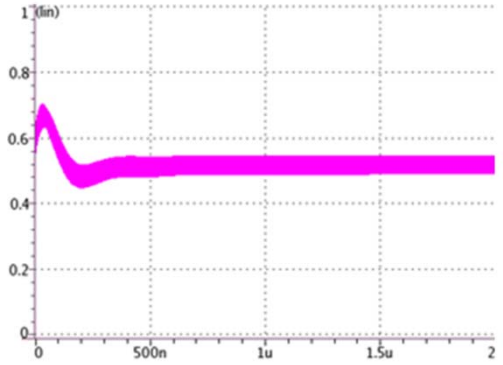
**VCO phase noise simulation**




**Frequency tuning range**

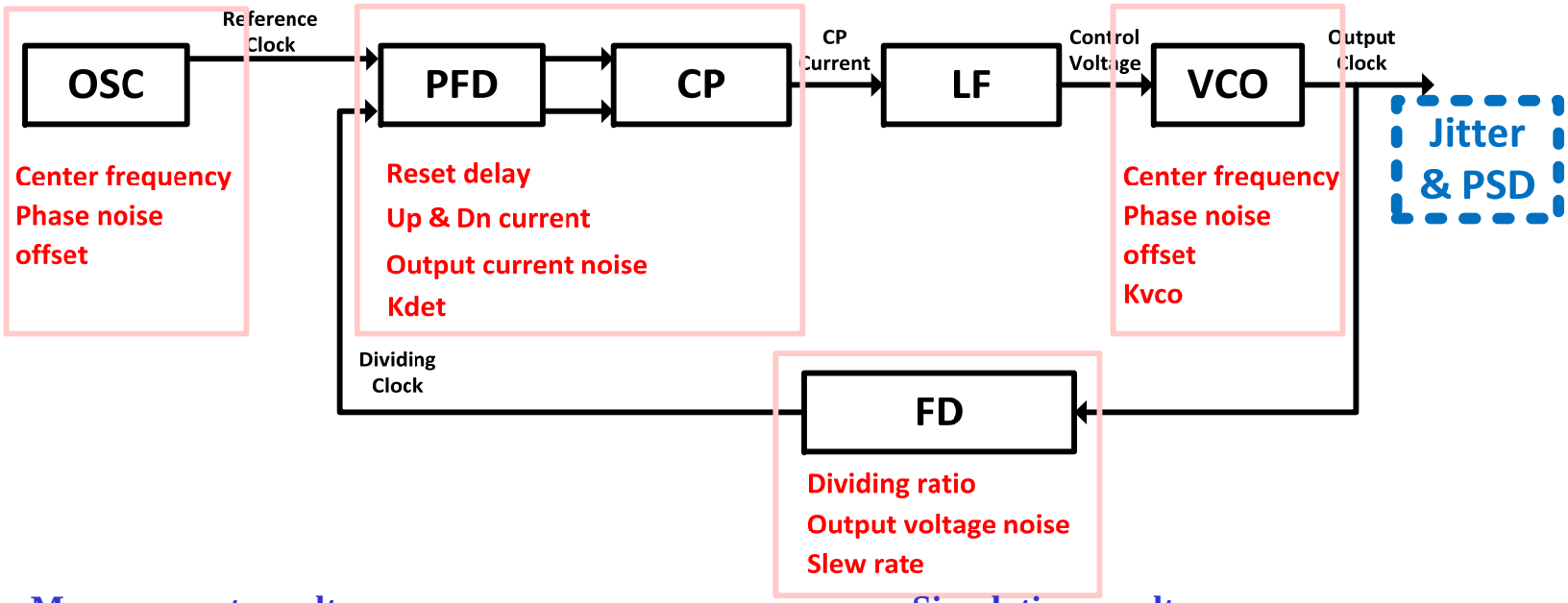



**PLL locking behavior**

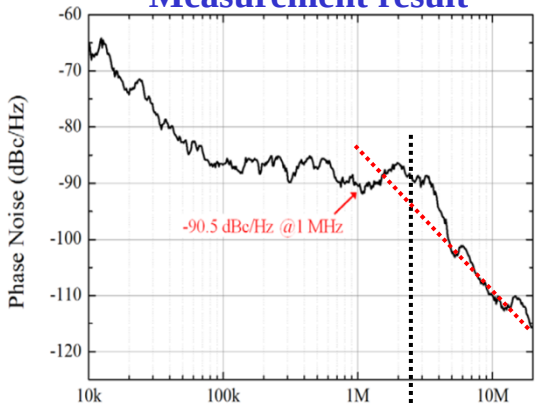


# Jitter Analysis with Behavioral Simulation

## Behavioral simulation block diagram

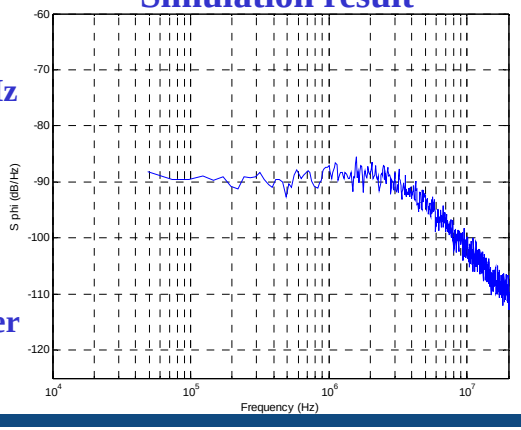



## Measurement result




- VCO
  → 350-MHz, -84 dBc/Hz @ 1-MHz offset
- Loop bandwidth
  → 2.5-MHz
- Reference input jitter
  → 8-ps
- Phase noise integrated jitter
  → 47-ps

## Simulation result




- VCO
  → 350-MHz, -86 dBc/Hz @ 1-MHz offset
- Loop bandwidth
  → 2.5-MHz
- RMS Jitter : 48.8-ps
  → VCO only : 28-ps
  → PFD_CP only : 40-ps