제23회 한국반도체학술대회
The 23rd Korean Conference on Semiconductors

대회개요 프로그램 초록제출 초록발표 참가등록 전시/후원 장소/숙박 커뮤니티

• 등록안내 • 온라인등록

D- -4

초록접수마감 2015.11.20(금)
~~2015.11.13(금)~~
초록채택통보 2015.12.23(수)
~~2015.12.18(금)~~
사전등록마감 2016.01.29(금)

모집분야 프로그램
초록작성 숙박안내
사전등록 뉴스레터
Call for Paper Call for Participatio

공지사항

KCS 2016에 대한 최근 소식

- 온라인 등록시스템이 오픈되었습니다.
- 온라인 초록접수가 성황리에 마감되었습니다.
- 호텔/리조트 예약은 12월 1일부터 가능합니다.
- Tentative Program이 업데이트 되었습니다.

친구 중 제일 먼저 좋아요를 클릭하세요

KCS
2015년 12월 23일

제23회 한국반도체학술대회 사무국입니다.
오늘은 크리스마스 이브입니다.
모두 행복 가득하고, 따뜻한 크리스마스 보내시길 바랍니다.^^
**초록채택통보는 12월 23일~24일 개별 메일로 통보진행되었으니
확인을 부탁 드립니다.... 더 보기

주관 성균관대학교 SUNGKYUNKWAN UNIVERSITY | KSIA 한국반도체산업협회 | SAR 한국반도체연구조합

주최 KPS 한국물리학회 The Korean Physical Society | MRS 한국재료학회 Materials Research Society of Korea | 대한전기학회 | IEIE 대한전자공학회 The Institute of Electronics and Information Engineers | IDEC 반도체설계교육센터 IC DESIGN EDUCATION CENTER

후원 GWCVB 강원컨벤션뷰로 | SAMSUNG | SK 하이닉스 | 동부하이텍 Dongbu HiTek

FAQ
자주 묻는 질문과 답변

1. 논문은 몇 번 제출하나요?
2. 사무국 연락처는 무엇인가요?

[제23회 한국반도체학술대회_Program at a Glance]

2월 22일(월)	Room A 태백룸(5층)	Room B 함백룸(5층)
14:00-18:00	[Short Course 1] 3차원 집적 기술: 원리와 응용	[Short Course 2] 차세대 저전력소자의 개발과 설계

2월 23일(화)	Room A	Room B	Room C	Room D	Room E	Room F	Room G	Room H	Room I	Room J	Room K	Room L
			5층			6층						5층
	태백I	태백II+III	함백I	함백II+III	컨벤션홀L	봉래I	봉래II+III	옥백I	옥백II	청옥I	청옥II+III	로비
08:30-10:30	[TA1-L] Analog Design I	[TB1-D] 1D/2D Materials & Devices	[TC1-F] Novel Si Devices and Integrated Circuits (4)	[TD1-G] Device Physics and Characterization 1 : Field-effect		[TF1-I] High efficiency sensors and devices	[TG1-F] Novel Si Devices and Integrated Circuits (1)	[TH1-J] Nanofabrication for Application		[TJ1-K] Memory processing and RRAM operation	[TK1-R] Interaction of system SW and semiconductor	
10:30-10:40	휴식 (& 커피, 다과)											
10:40-12:40	[TA2-L] Analog Design II	[TB2-D] Oxide Semiconductors	[TC2-M] RFIC and smart RFID tags	[TD2-G] Reliability Analysis : Thin-film transistors and field-effect transistors		[TF2-O] VLSI System Design for Communications	[TG2-F] Novel Si Devices and Integrated Circuits (2)	[TH2-J] Nanofabrication for Application	CDC	[TJ2-K] NAND, PCRAM, and MRAM	[TK2-R] Little more faster, and even better reliability	
12:40-13:40	점심 [포레스트볼룸 / 4층]											Chip Design Contest & 전시
13:40-14:20	기조강연 1 : Prof. Akira Toriumi (The University of Tokyo) "Materials Innovation for Versatile Electron Devices in IoT Era" [컨벤션홀 K+W / 5층]											
14:20-15:00	기조강연 2 : 박재근 교수 (한양대학교) " Nonvolatile Memory Technology beyond 20nm : Dilemma & Challenge" [컨벤션홀 K+W / 5층]											
15:00-15:10	휴식 (& 커피, 다과)											
15:10-17:10	[TA3-A] A2: Enabling packaging technologies	[TB3-D] Process Technology for Thin Films	[TC3-H] Display and Imaging Technologies	[TD3-G] Device Modeling and Simulation 1 : RF, teraherz, low-power, and		[TF3-Q] Metrology and Inspection I	[TG3-F] Novel Si Devices and Integrated Circuits (3)	[TH3-J] Graphene and Related Carbon Nanostructures	[TI1-N] Advances in Design Technology	[TJ3-K] Circuit related topics and memory selectors	[TK3-E] Advanced GaN Technology	
17:10-18:30					포스터 세션1 [TP1]							
18:30-20:00	만찬 [컨벤션홀 K+W / 5층]											
20:00-	Rump Session 1 : 스케일링 한계 극복을 위한 미래 반도체 기술 [태백룸 / 5층] Rump Session 2 : 초연결 사회의 반도체 기술 전망과 과제 [함백룸 / 5층]											

2월 24일(수)	Room A	Room B	Room C	Room D	Room E	Room F	Room G	Room H	Room I	Room J	Room K	Room L
			5층			6층						5층
	태백I	태백II+III	함백I	함백II+III	컨벤션홀L	봉래I	봉래II+III	옥백I	옥백II	청옥I	청옥II+III	로비
08:30-10:00	[WA1-A] A1: Contact and thin film technologies for high performance	[WB1-D] Thin Films for Emerging Devices I	[WC1-C] Materials Growth & Characterization : Emerging new electrical	[WD1-G] Device Physics and Characterization 2 : Memory devices		[WF1-Q] Metrology and Inspection II	[WG1-F] Materials and Processing Technologies	[WH1-J] Two-Dimensional Materials beyond Graphene	[WI1-N] Architecture-Level Design Techniques	[WJ1-K] Unconventional approaches in memory research	[WK1-E] GaN Power Device	
10:00-10:10	휴식 (& 커피, 다과)											
10:10-11:40	[WA2-A] A3: Novel interconnect and packaging technologies for emerging	[WB2-D] Thin Films for Emerging Devices II	[WC2-C] Materials Growth & Characterization : III-Nitrides and Si	[WD2-G] Device Modeling and Simulation 2 : Ab-initio and theoretical study		[WF2-O] VLSI System Design and Applications	[WG2-F] Si and Group-IV Photonics	[WH2-J] Two-Dimensional Materials / Spintronics	[WI2-B] Patterning	[WJ2-P] Device for Energy (Solar Cell, Power Device, Battery, etc.)	[WK2-E] III-V Device	전시
11:40-13:00					포스터 세션2 [WP1]							
13:00-	점심 [포레스트볼룸 / 4층]											

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제23회 한국반도체학술대회
2016년 2월 22일(월)-24일(수), 강원도 하이원리조트

L. Analog Design 분과

Room A
태백 I (5층)

2016년 2월 23일(화) 10:40-12:40
[TA2-L] Analog Design II
좌장 : 박재진(삼성전자)

TA2-L-1	10:40-10:55	**A 1.2 V CMOS-based Temperature Sensor in the Subthreshold Operation** Woosul Shin, Jun-Seok Na, Bong-Choon Kwak, Seong-Kwan Hong, and Oh-Kyong Kwon *Department of Electronic Engineering, Hanyang University*
TA2-L-2	10:55-11:10	**SIDO DC-DC 컨버터의 부하 범위 확장을 위한 cross regulation 감쇠 방법** 정현수, 홍요한, 팜응옥손, 백광현 *중앙대학교 전자전기공학과*
TA2-L-3	11:10-11:25	**Fast-transient Output-capacitorless LDO Regulator for SoC Applications** Eun-Taek Sung, Jeong-Yun Lee, Keum-Won Ha, Ye-Seul Baek, and Donghyun Baek *School of Electrical Engineering, Chung-Ang University*
TA2-L-5	11:40-11:55	**Design of a Transceiver Transmitting Power, Clock, and Data over a Single Optical Fiber for Future Automotive Network System** Woorham Bae and Deog-Kyoon Jeong *Department of Electrical and Computer Engineering, Seoul National University*
TA2-L-6	11:55-12:10	**A 3/6/12-Gb/s Multi-Rate Clock and Data Recovery Circuit with a Multi-Mode Rotational Bang-Bang Phase Detector** Ki-Hyun Pyun, Dae-Hyun Kwon, and Woo-Young Choi *Department of Electrical and Electronic Engineering, Yonsei University*

A 3/6/12-Gb/s Multi-Rate Clock and Data Recovery Circuit with a Multi-Mode Rotational Bang-Bang Phase Detector

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For many serial data communication applications such as display interface, multi-rate operation is required. For this, clock and data recovery (CDR) circuits have to operate for several different data rates. Implementing CDRs with wide tuning-rage VCOs is the most straight-forward approach, but it is very challenging to design a wide tuning-range VCO with constant VCO gain, which is required for CDR stability, over the required entire frequency band. We propose a new multi-rate CDR architecture based on a multi-mode rotational bang bang phase detector(MRBBPD), which can operate at 3, 6 and 12-Gbps. Fig. 1 shows the schematic of our CDR. The MRBBPD supports full-rate, half-rate, and quarter-rate phase detection operations enabling the multi-rate operation of the CDR without a wide tuning-range VCO. The MRBBPD is composed of eight DFFs, three rotational muxes, and two XOR gates and requires 8-phase clock signals from VCO. The rotational muxes produce different output signals depending whether it is in the full-rate, half-rate, or quarter-rate mode as shown in the timing diagram given in Fig. 1(b). Fig. 1(c) shows the 65-nm CMOS post-layout simulated eye-diagrams of the recovered data for 2^7-1 PRBS input data at three different data rates of 3Gb/s, 6Gb/s and 12Gb/s. Data recover is successfully done. Compared to conventional quarter-rate CDR, our CDR has less six XORs and three charge-pumps, which results in significant reduction of power consumption and area occupation.

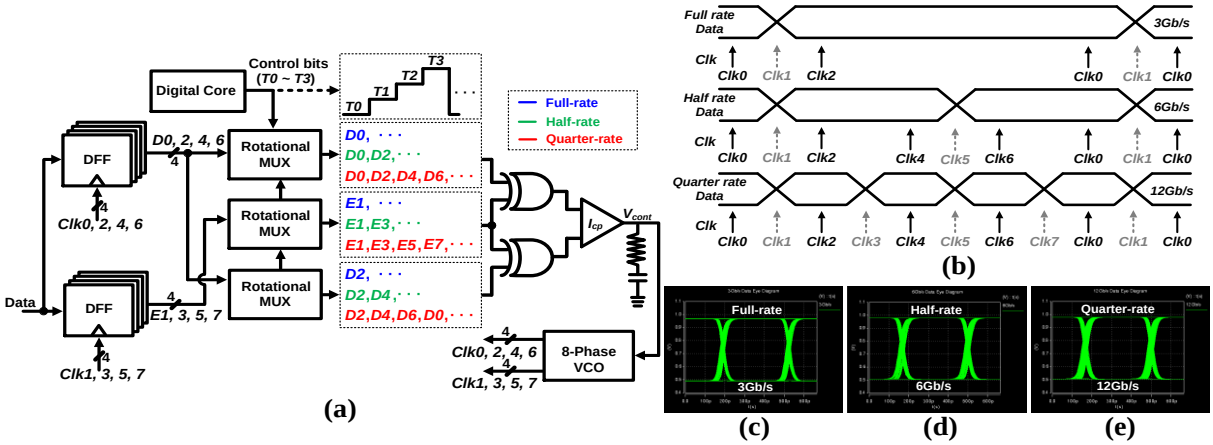

Fig. 1. (a) Block diagram of MRBBPD (b) Timing diagram of Full/Half/Quarter-rate operation (c) Eye diagram of 3Gb/s (d) Eye diagram of 6Gb/s (e) Eye diagram of 12Gb/s